FIG. 3

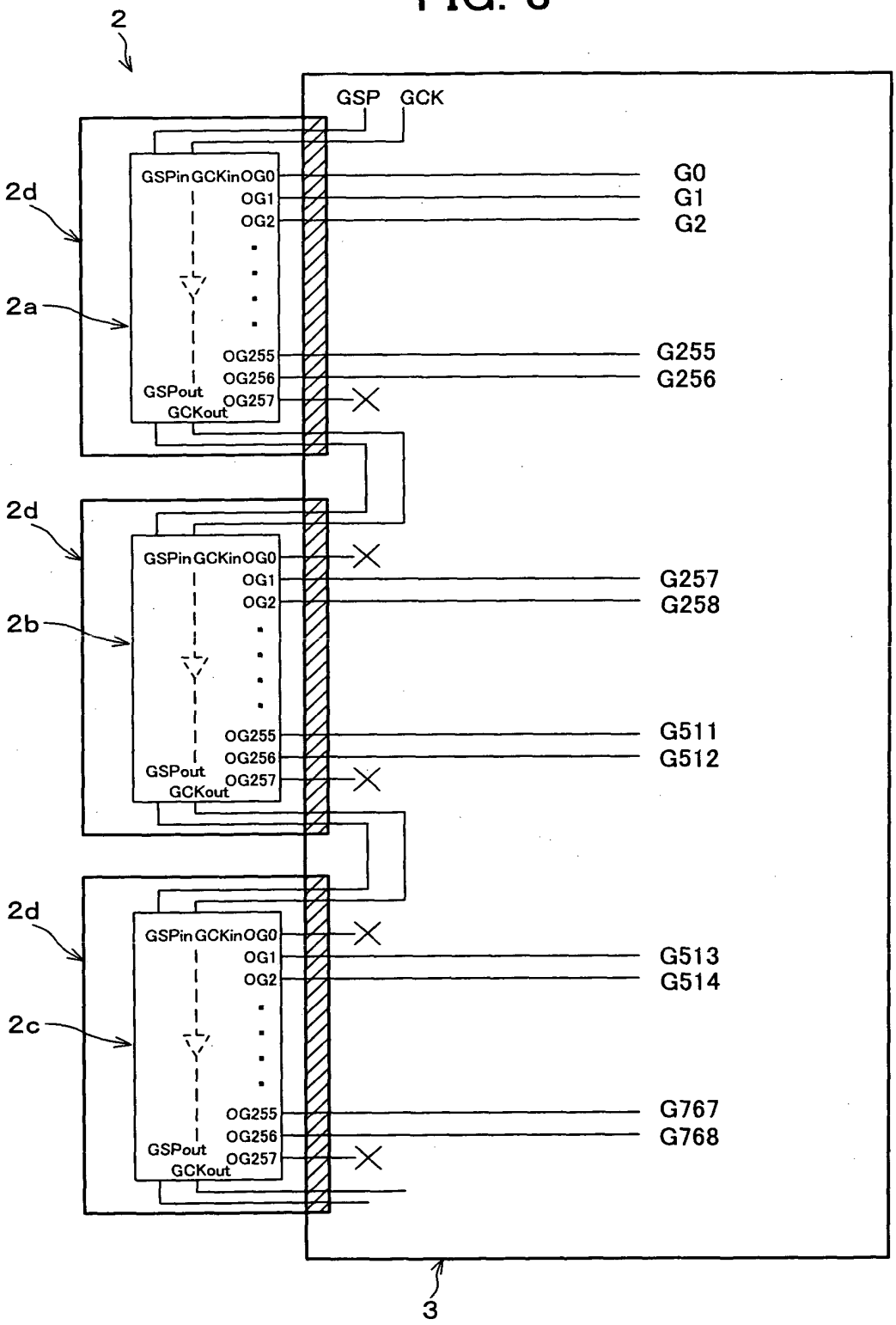

2
GSP
GCK
2d
2a
GSPin
GCKin
OG0
OG1
OG2
OG255
OG256
OG257
GSPout
GCKout
G0
G1
G2
G255
G256
2d
2b
G257
G258
G511
G512
2d
2c
G513
G514
G767
G768
3

FIG. 4

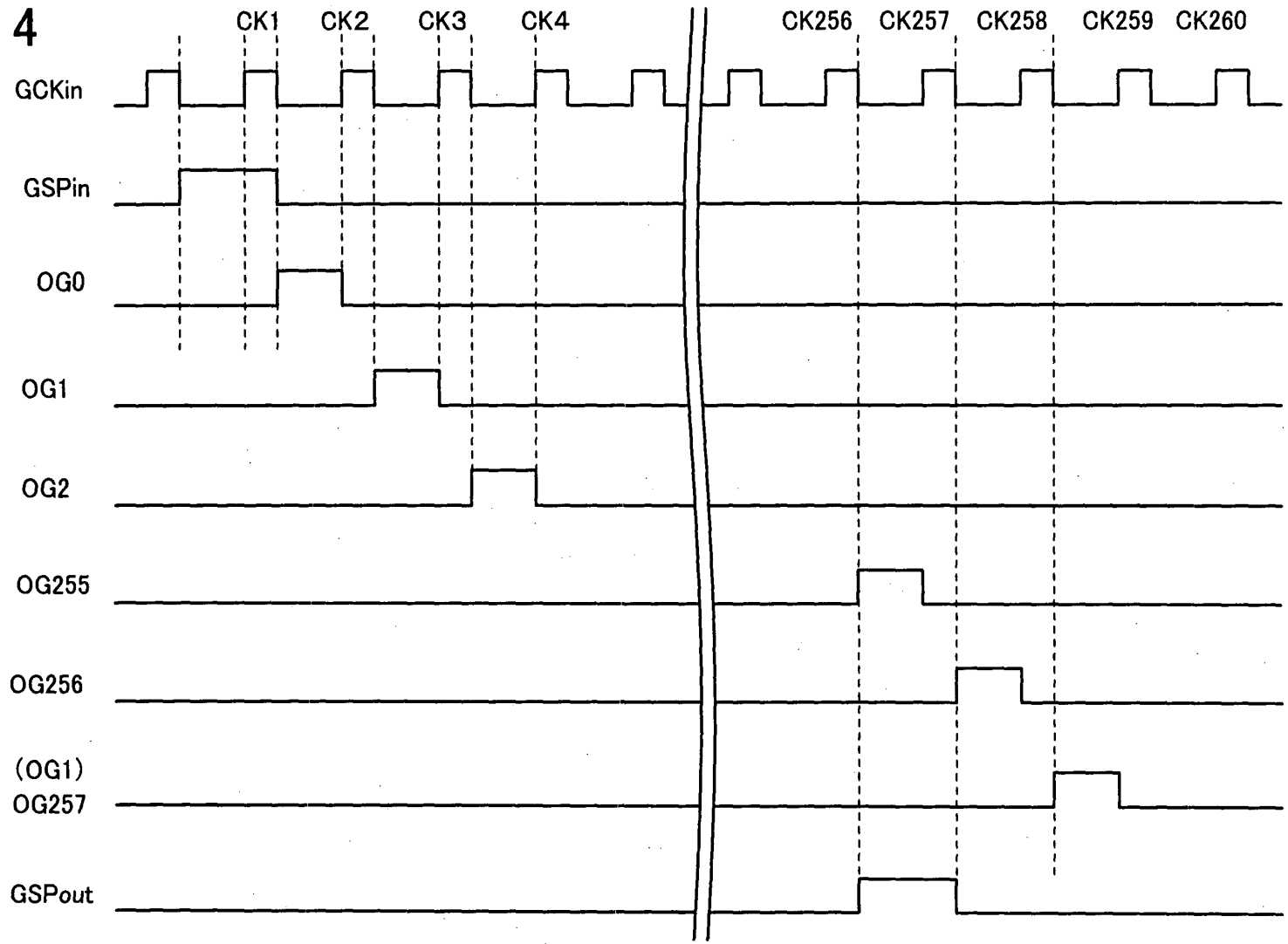

CK1
CK2
CK3
CK4
CK256
CK257
CK258
CK259
CK260
GCKin
GSPin
OG0
OG1
OG2
OG255
OG256
(OG1)
OG257
GSPout

FIG. 5

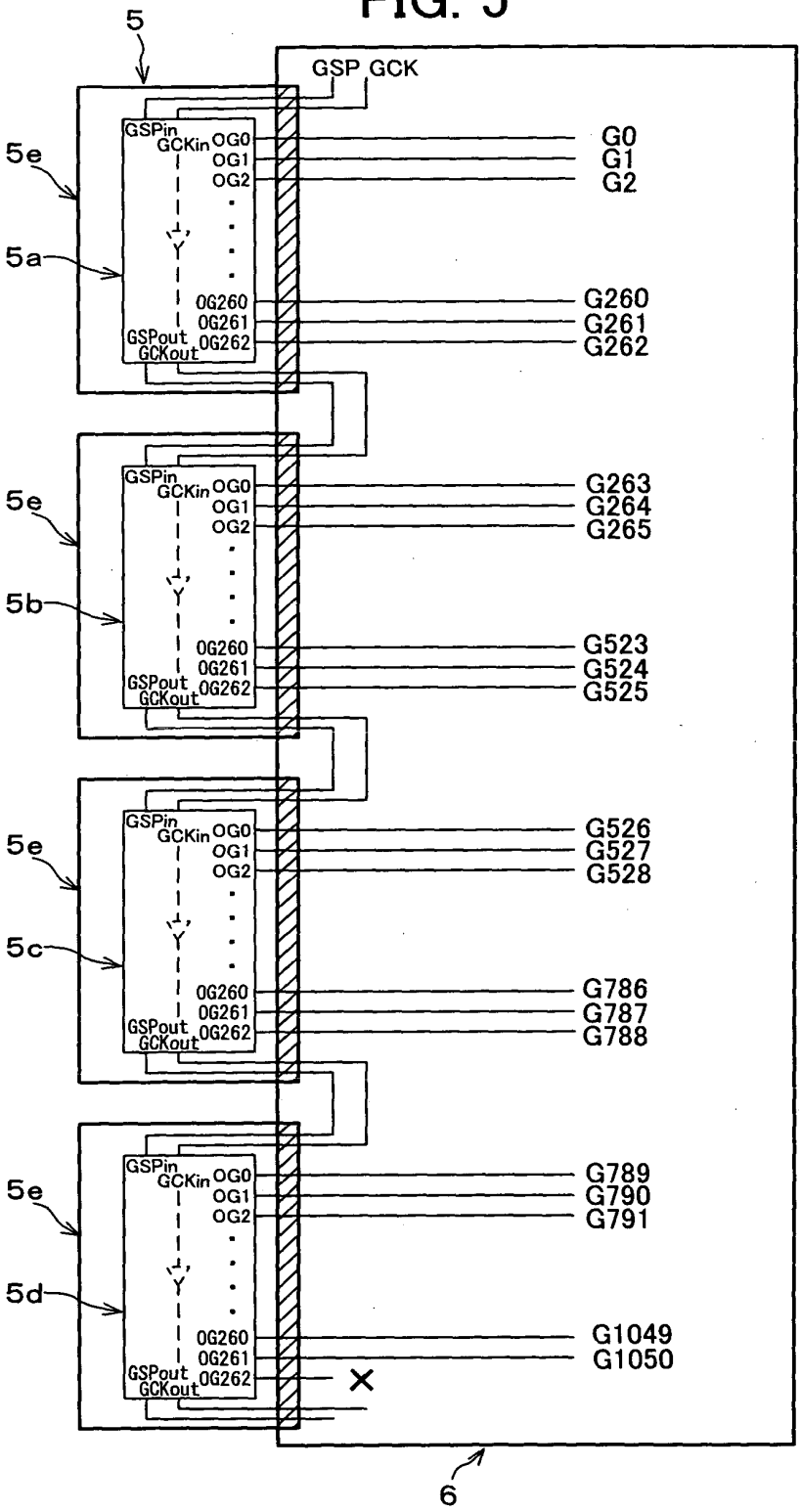

5
GSP GCK
5e
5a
GSPin
GCKin
OG0
OG1
OG2
Y
OG260
OG261
GSPout
GCKout
OG262
G0
G1
G2
G260
G261
G262
5e
5b
G263
G264
G265
G523
G524
G525
5e
5c
G526
G527
G528
G786
G787
G788
5e
5d
G789
G790
G791
G1049
G1050
6

FIG. 6

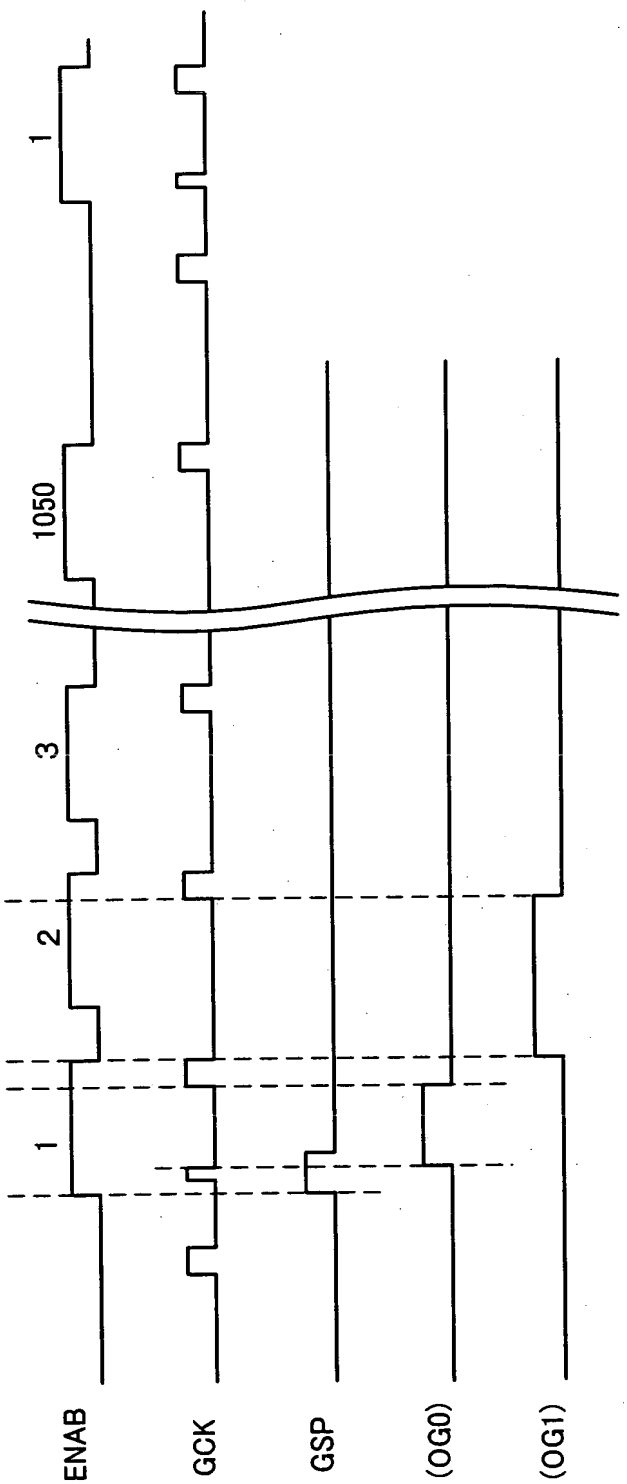


FIG. 7

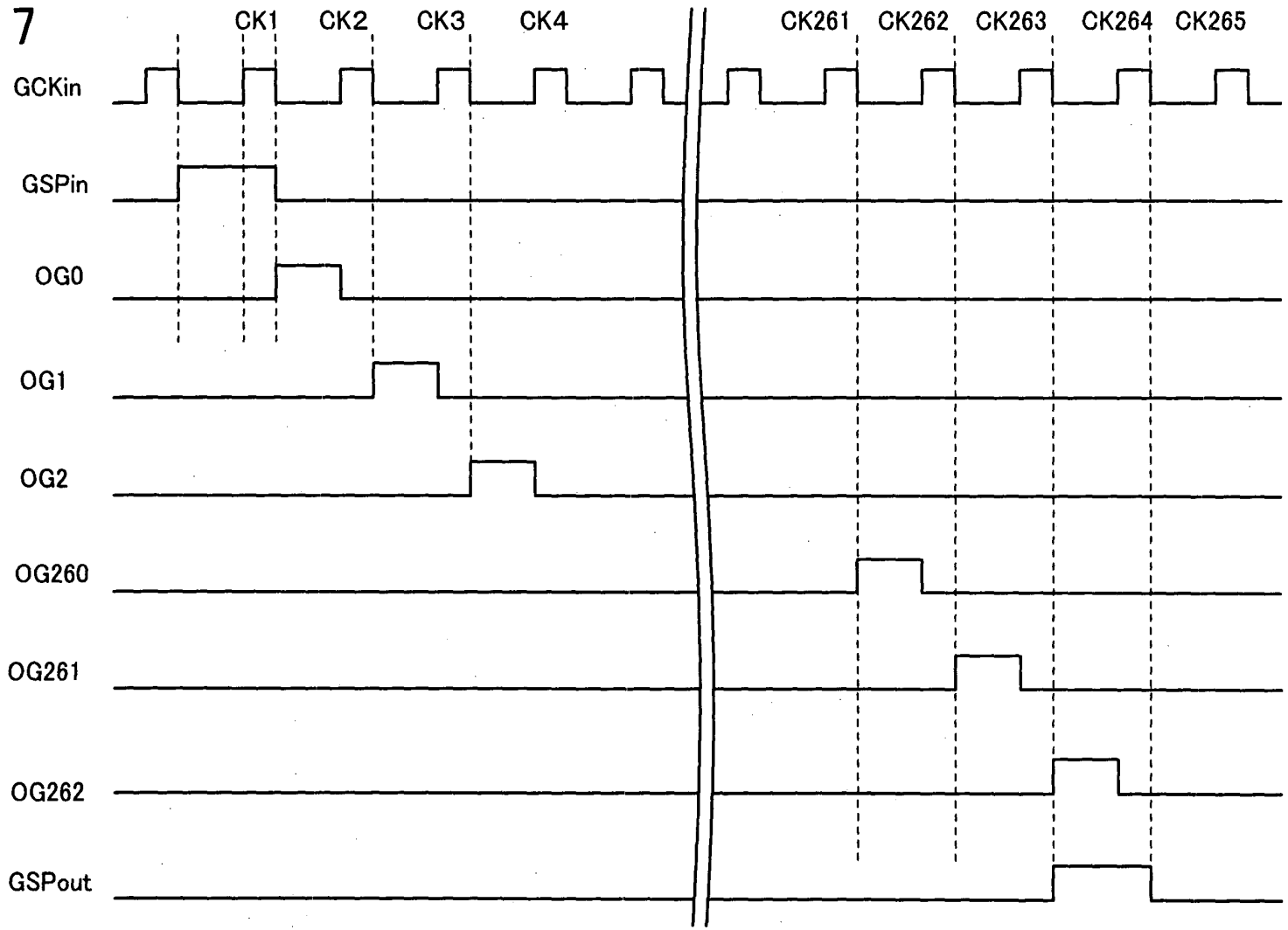

CK1
CK2
CK3
CK4
CK261
CK262
CK263
CK264
CK265
GCKin
GSPin
OG0
OG1
OG2
OG260
OG261
OG262
GSPout

FIG. 8

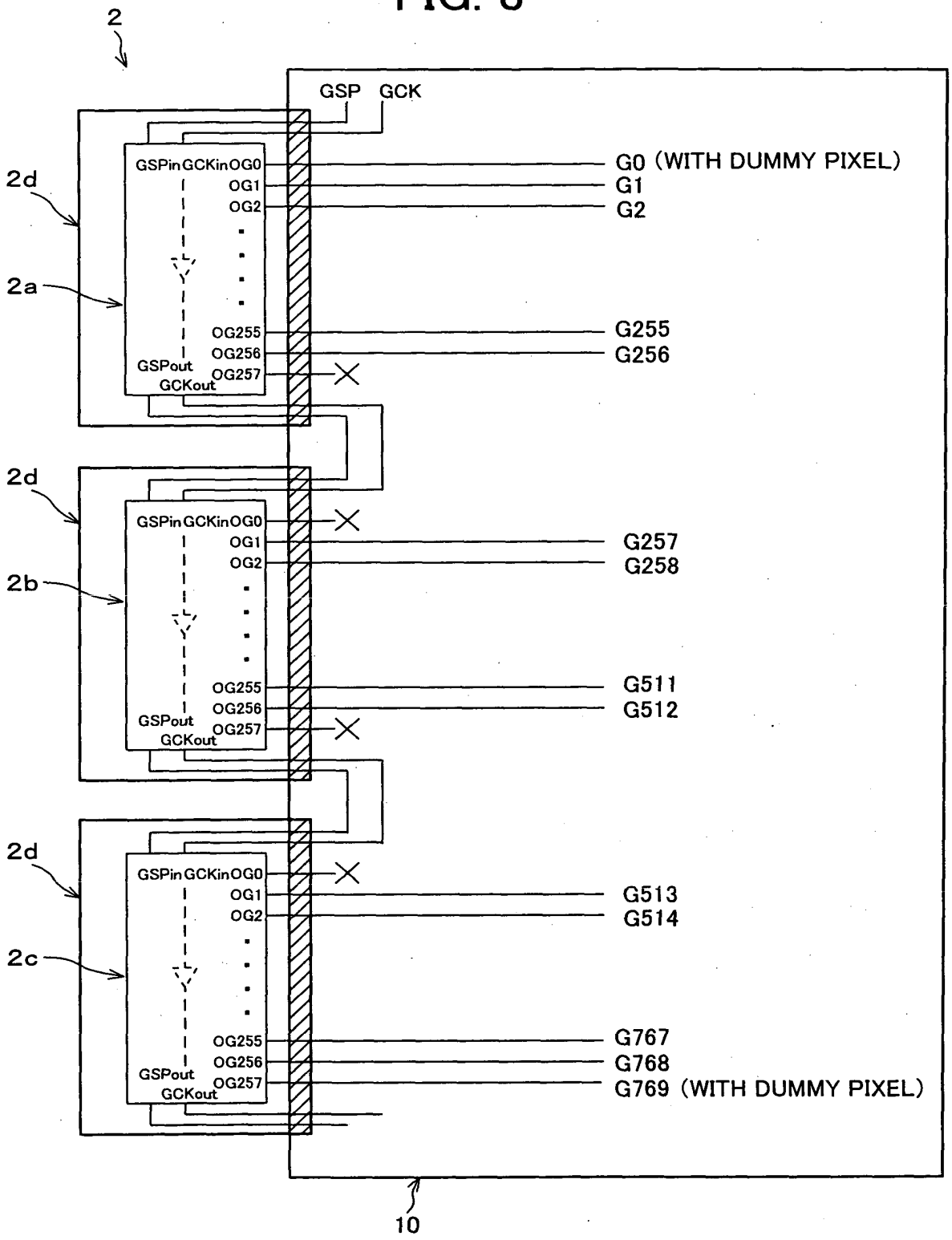

2
GSP
GCK
2d
2a
GSPin
GCKin
OG0
OG1
OG2
OG255
OG256
OG257
GSPout
GCKout
G0 (WITH DUMMY PIXEL)
G1
G2
G255
G256
2d
2b
G257
G258
G511
G512
2d
2c
G513
G514
G767
G768
G769 (WITH DUMMY PIXEL)
10

FIG. 9

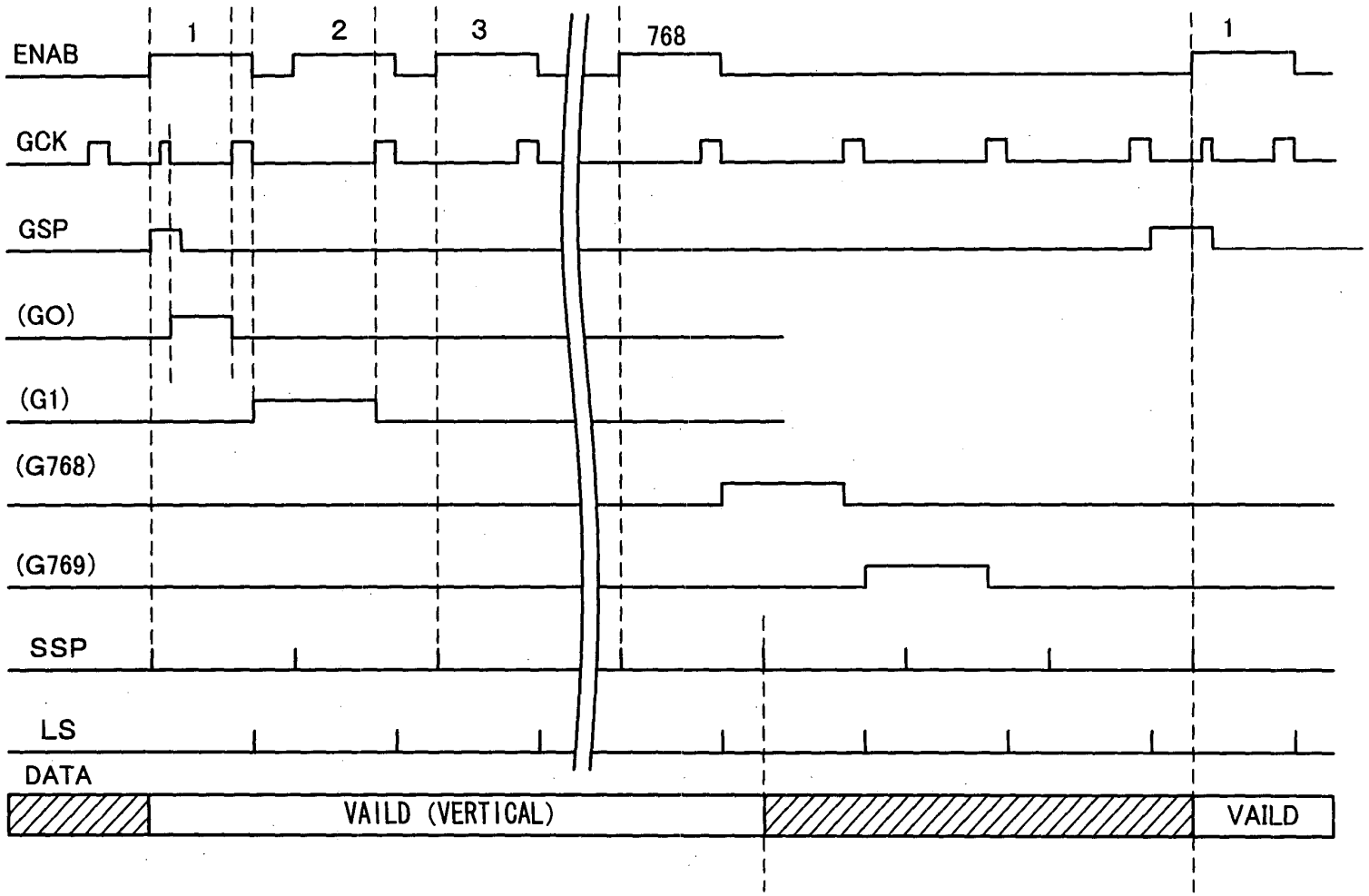

1
2
3
768
1
ENAB
GCK
GSP
(GO)
(G1)
(G768)
(G769)
SSP
LS
DATA
VAILD (VERTICAL)
VAILD

FIG. 10

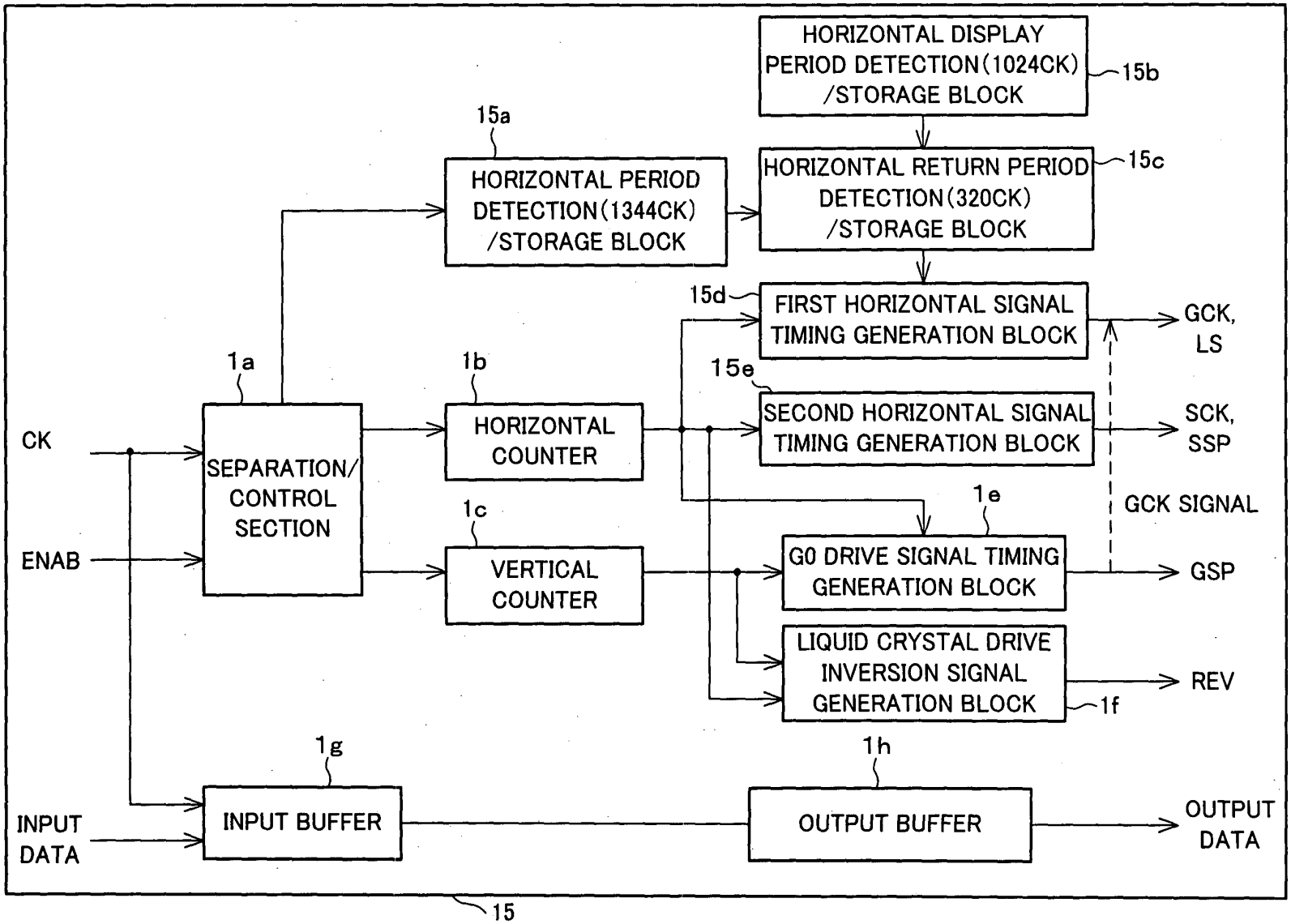

HORIZONTAL DISPLAY PERIOD DETECTION(1024CK) /STORAGE BLOCK
15b
15a
HORIZONTAL PERIOD DETECTION(1344CK) /STORAGE BLOCK
HORIZONTAL RETURN PERIOD DETECTION(320CK) /STORAGE BLOCK
15c
15d
FIRST HORIZONTAL SIGNAL TIMING GENERATION BLOCK
GCK, LS
1a
1b
15e
CK
SEPARATION/ CONTROL SECTION
HORIZONTAL COUNTER
SECOND HORIZONTAL SIGNAL TIMING GENERATION BLOCK
SCK, SSP
1e
GCK SIGNAL
1c
ENAB
VERTICAL COUNTER
G0 DRIVE SIGNAL TIMING GENERATION BLOCK
GSP
LIQUID CRYSTAL DRIVE INVERSION SIGNAL GENERATION BLOCK
REV
1f
1g
1h
INPUT DATA
INPUT BUFFER
OUTPUT BUFFER
OUTPUT DATA
15

FIG. 11

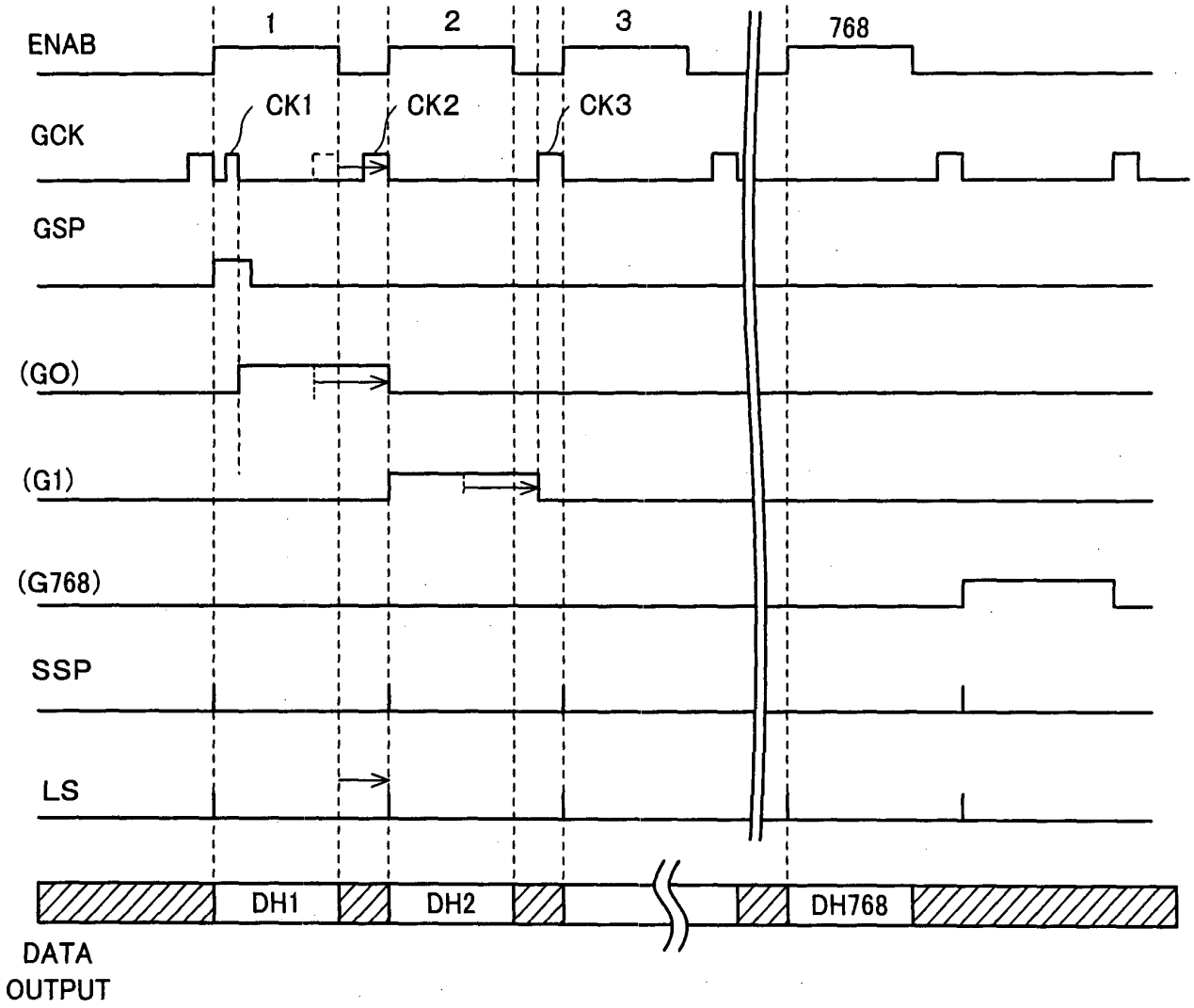

1
2
3
768
ENAB
CK1
CK2
CK3
GCK
GSP
(GO)
(G1)
(G768)
SSP
LS
DH1
DH2
DH768
DATA
OUTPUT

FIG. 12

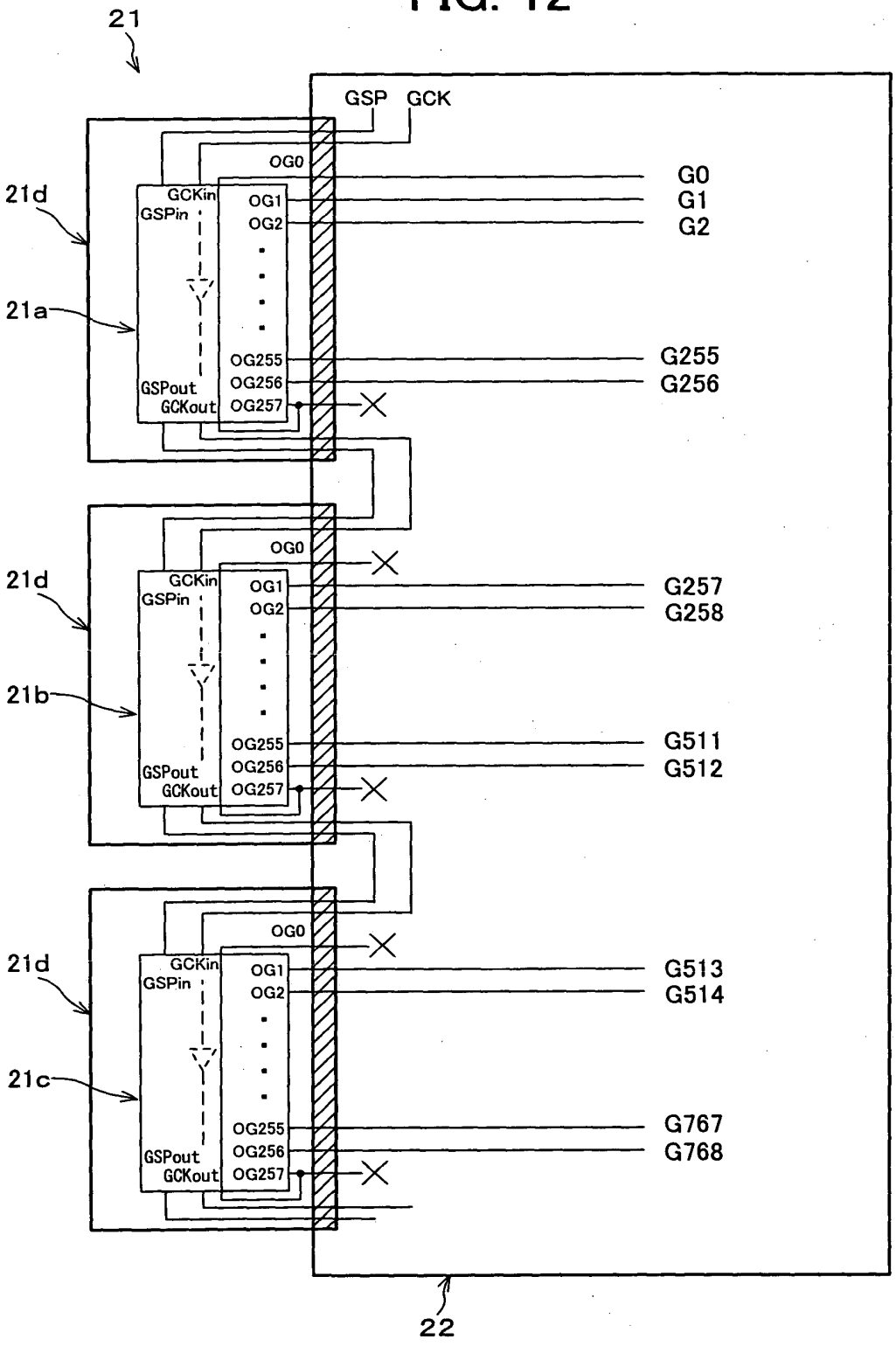

21
GSP
GCK
21d
21a
21b
21c
GCKin
GSPin
GSPout
GCKout
OG0
OG1
OG2
OG255
OG256
OG257
G0
G1
G2
G255
G256
G257
G258
G511
G512
G513
G514
G767
G768
22

FIG. 13

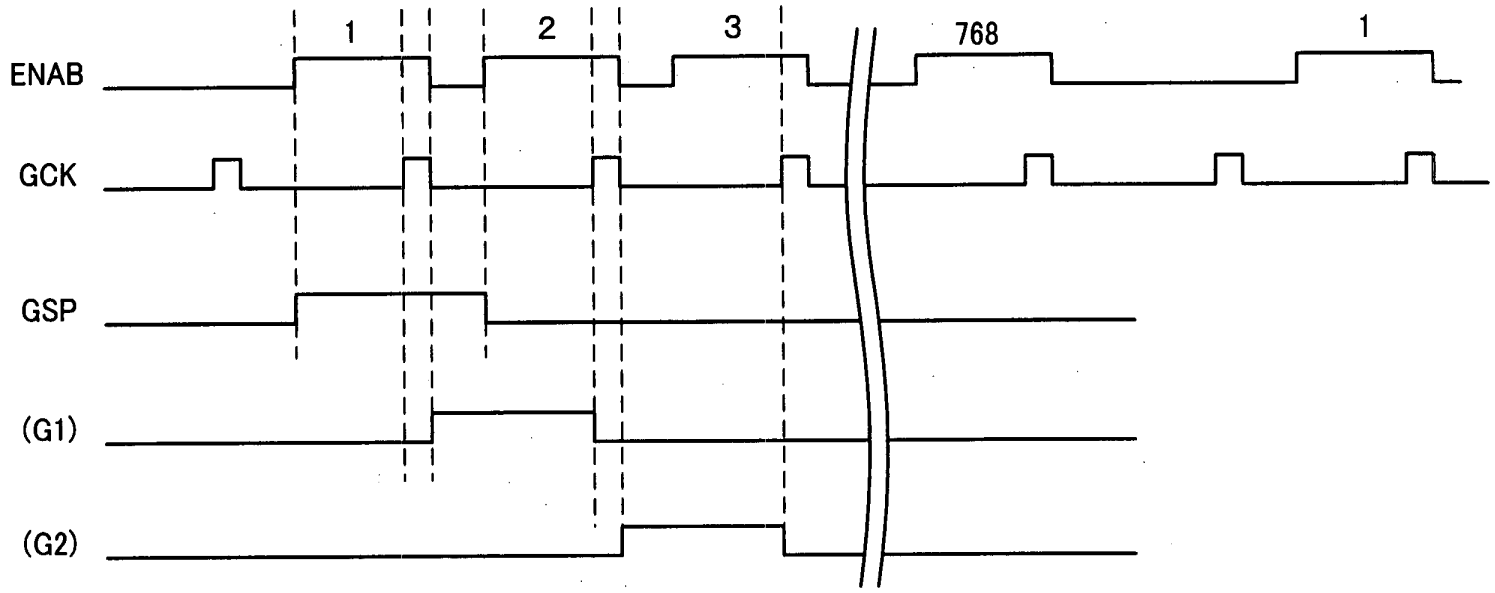


FIG. 14

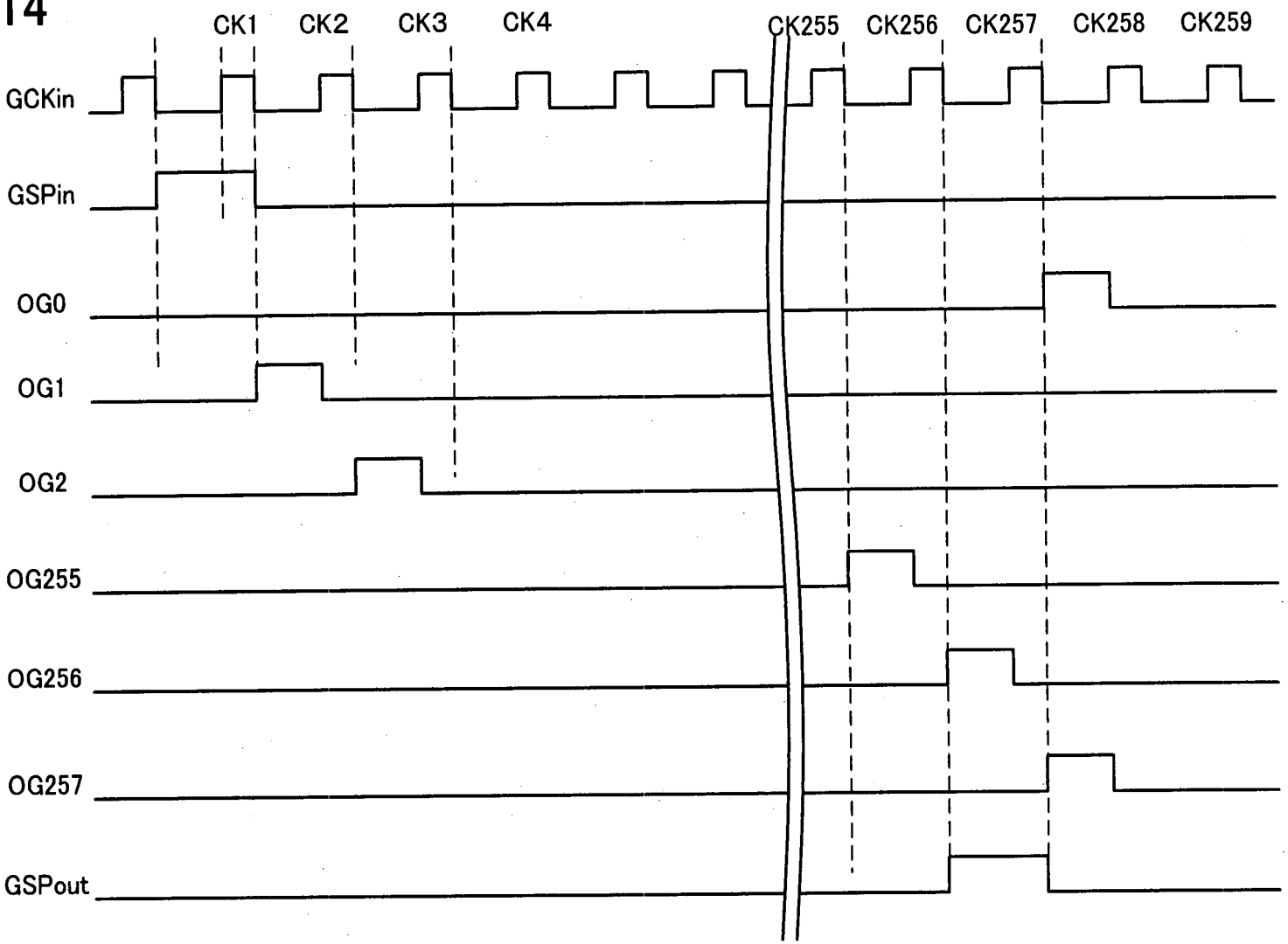

CK1
CK2
CK3
CK4
CK255
CK256
CK257
CK258
CK259
GCKin
GSPin
OG0
OG1
OG2
OG255
OG256
OG257
GSPout

FIG. 15

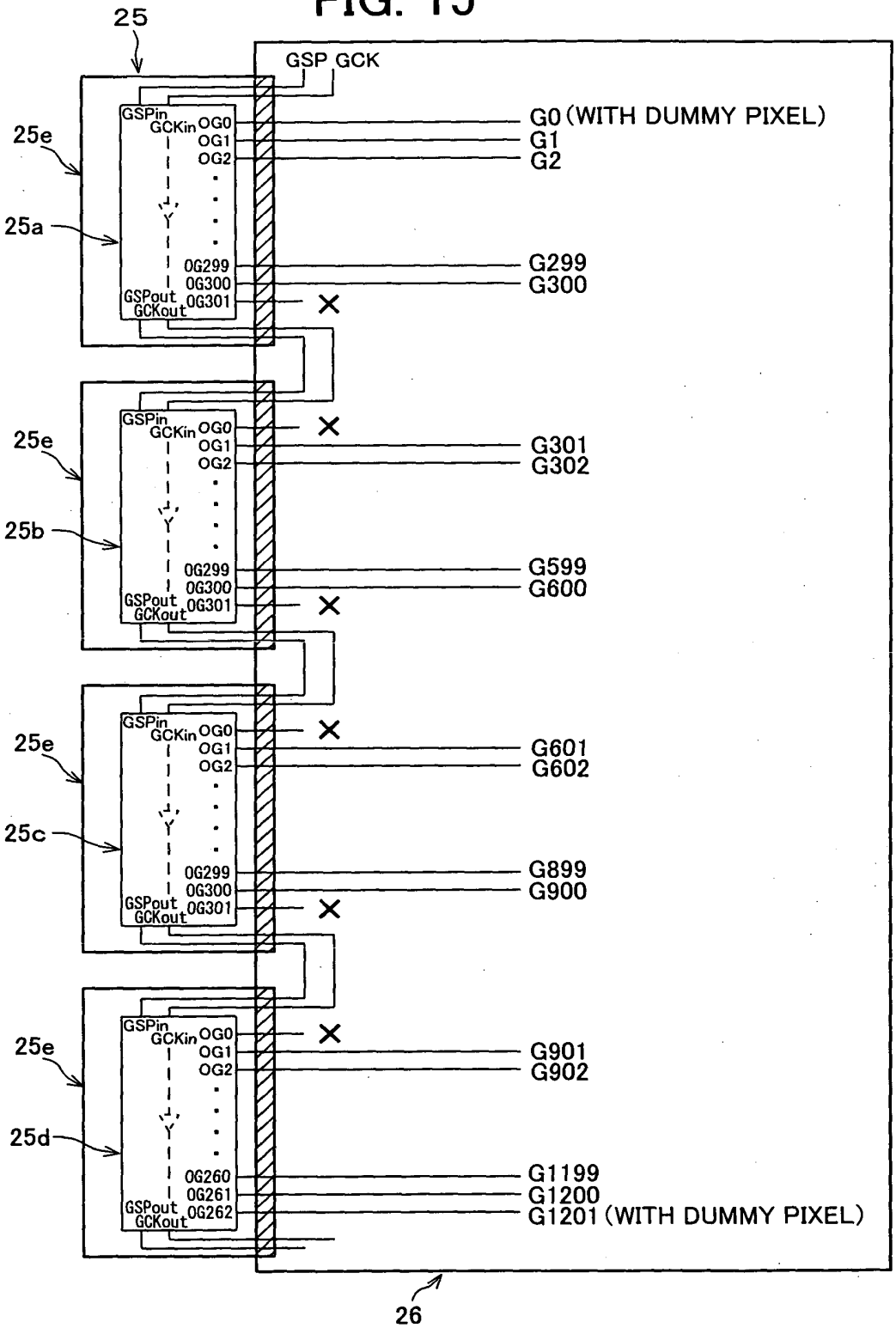

25
GSP GCK
25e
25a
25e
25b
25e
25c
25e
25d
GSPin
GCKin
OG0
OG1
OG2
Y
OG299
OG300
GSPout
GCKout
OG301
OG260
OG261
OG262
G0 (WITH DUMMY PIXEL)
G1
G2
G299
G300
G301
G302
G599
G600
G601
G602
G899
G900
G901
G902
G1199
G1200
G1201 (WITH DUMMY PIXEL)
26

FIG. 16

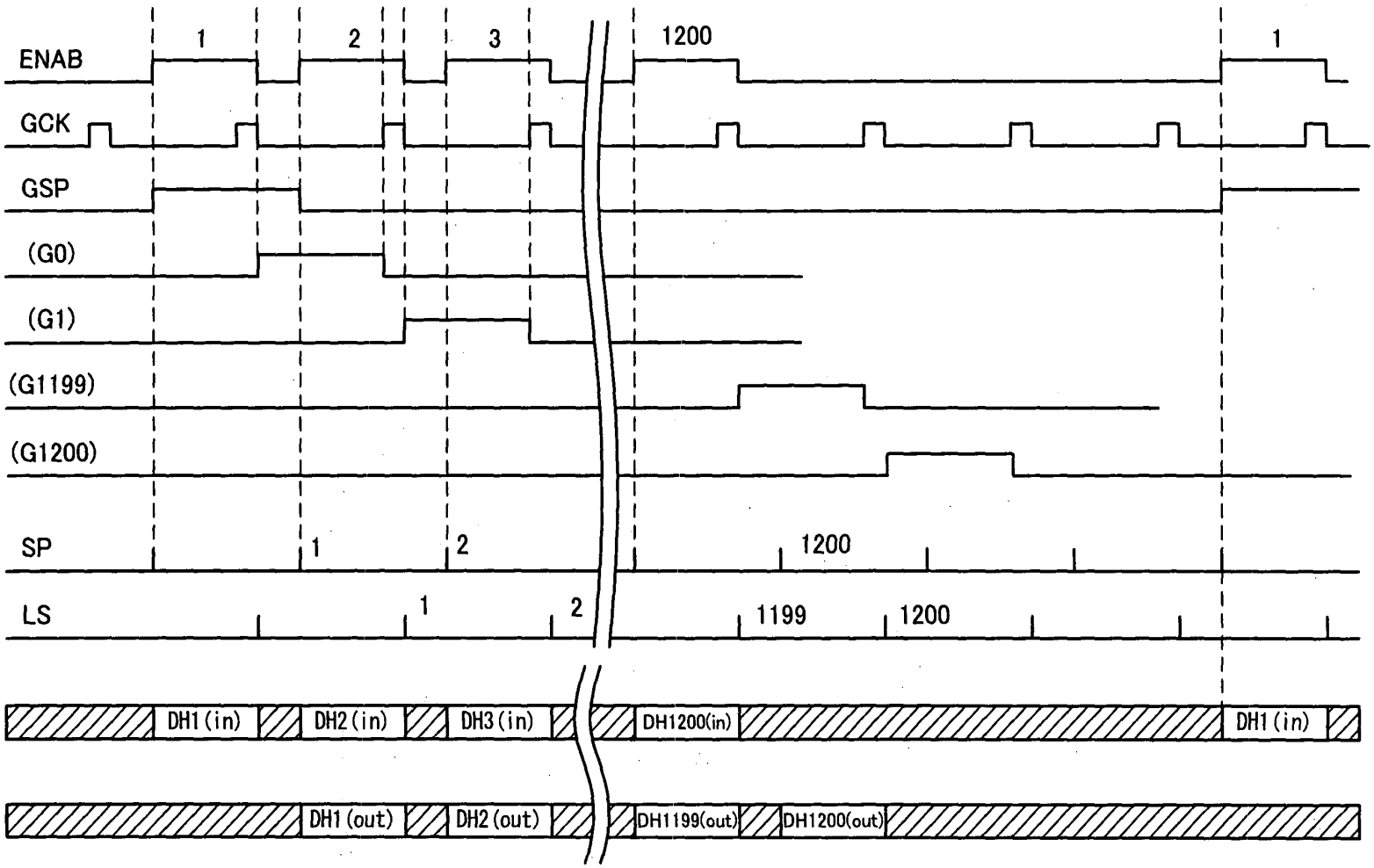

1
2
3
1200
1
ENAB
GCK
GSP
(G0)
(G1)
(G1199)
(G1200)
SP
1
2
1200
LS
1
2
1199
1200
DH1 (in)
DH2 (in)
DH3 (in)
DH1200(in)
DH1 (in)
DH1 (out)
DH2 (out)
DH1199(out)
DH1200(out)

FIG. 17

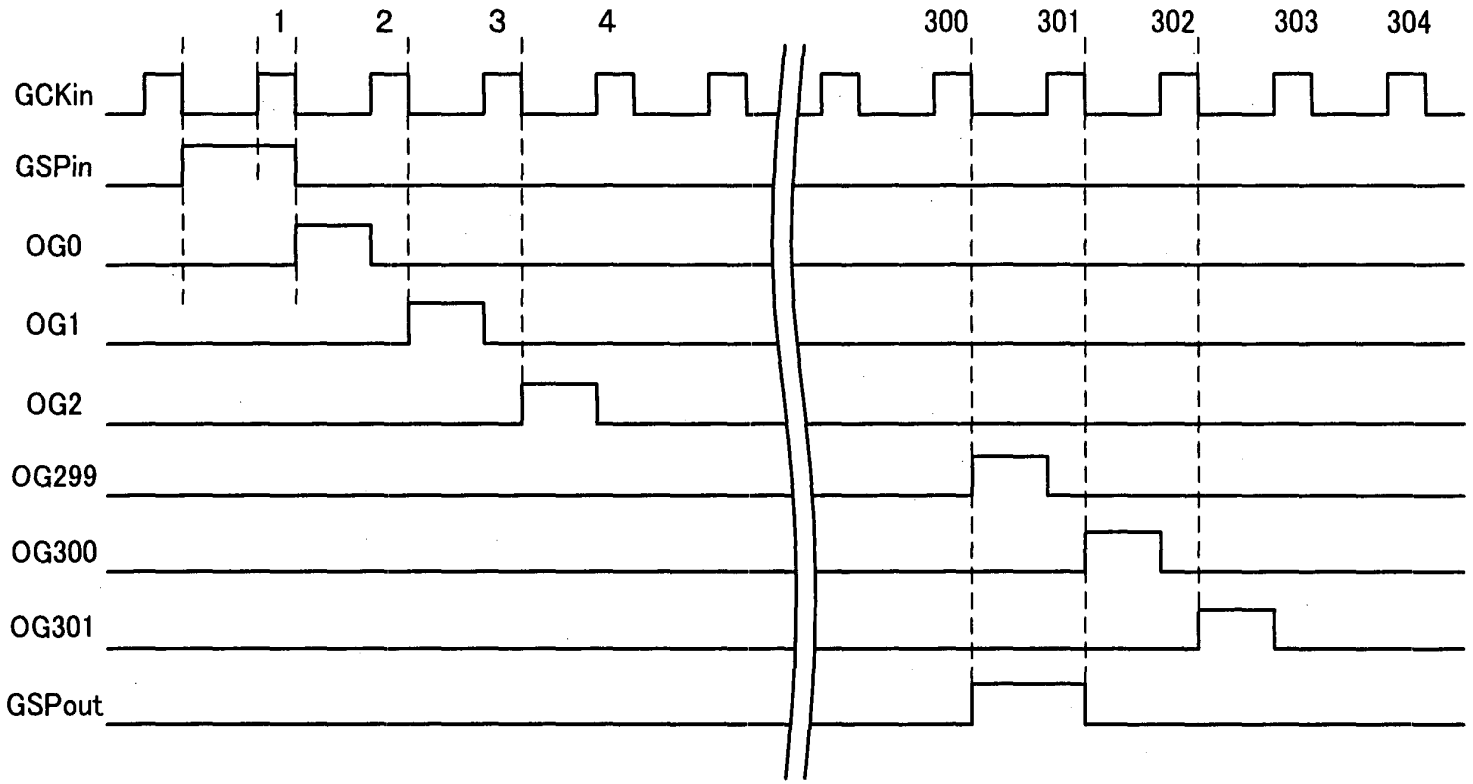

1
2
3
4
300
301
302
303
304
GCKin
GSPin
OG0
OG1
OG2
OG299
OG300
OG301
GSPout

FIG. 18

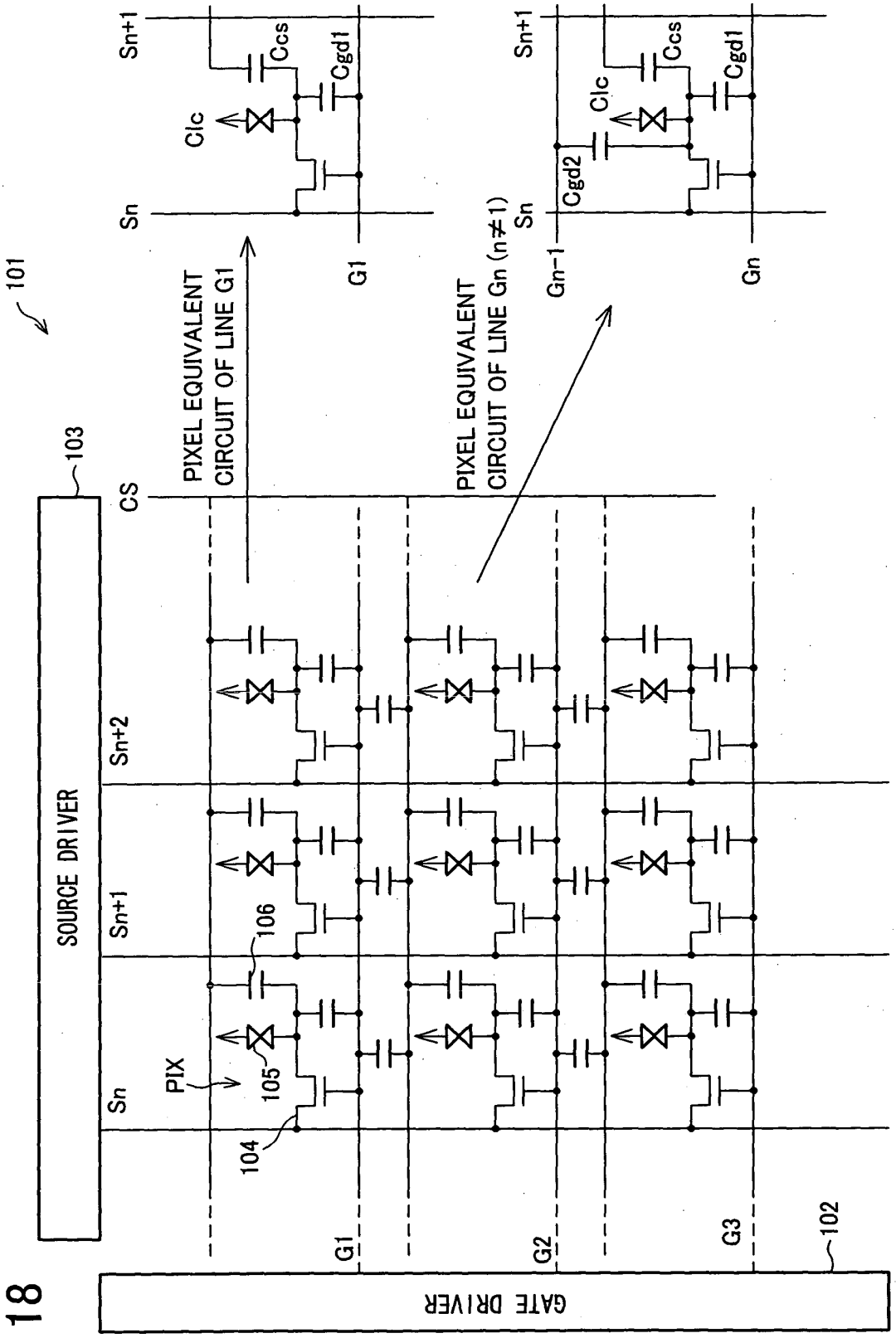

101
SOURCE DRIVER
103
GATE DRIVER
102
CS
Sn
Sn+1
Sn+2
PIX
104
105
106
G1
G2
G3
PIXEL EQUIVALENT CIRCUIT OF LINE G1
PIXEL EQUIVALENT CIRCUIT OF LINE Gn (n≠1)
Clc
Ccs
Cgd1
Cgd2
Gn-1
Gn

FIG. 19

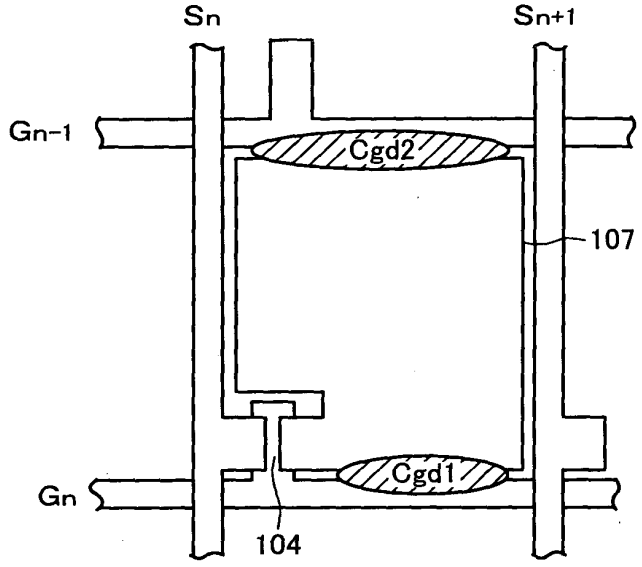

Sn
Sn+1
Gn-1
Cgd2
107
Gn
Cgd1
104

FIG. 20

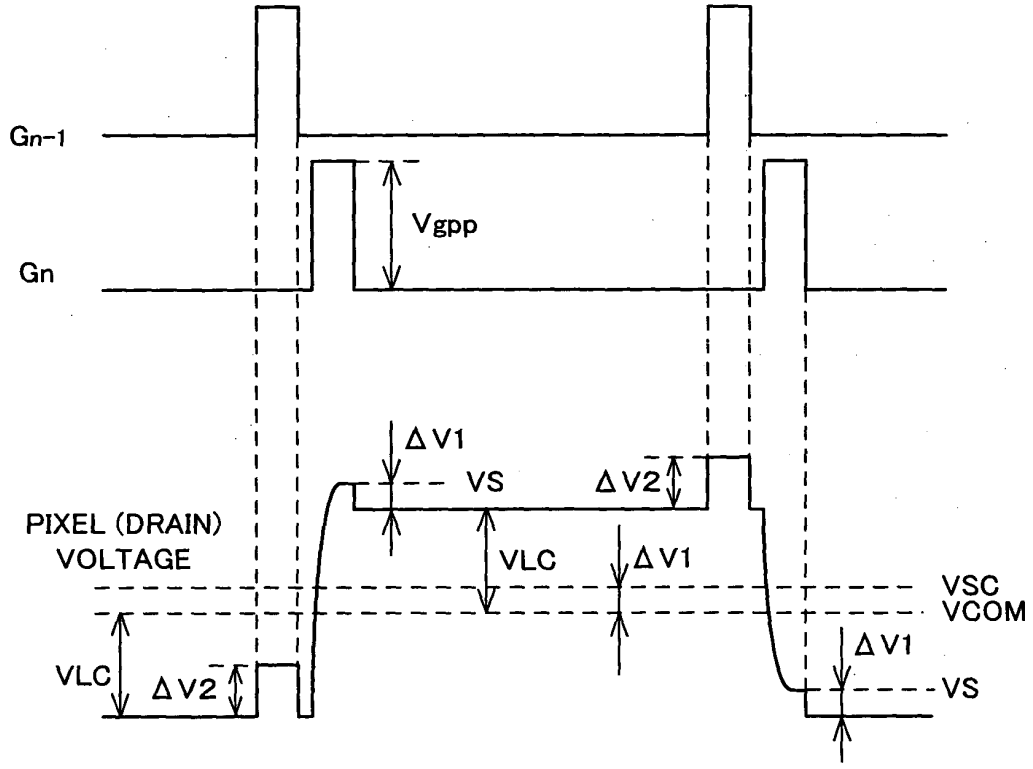

Gn-1
Vgpp
Gn
ΔV1
VS
ΔV2
PIXEL (DRAIN)
VOLTAGE
VLC
ΔV1
VSC
VCOM
VLC
ΔV2
ΔV1
VS

FIG. 21

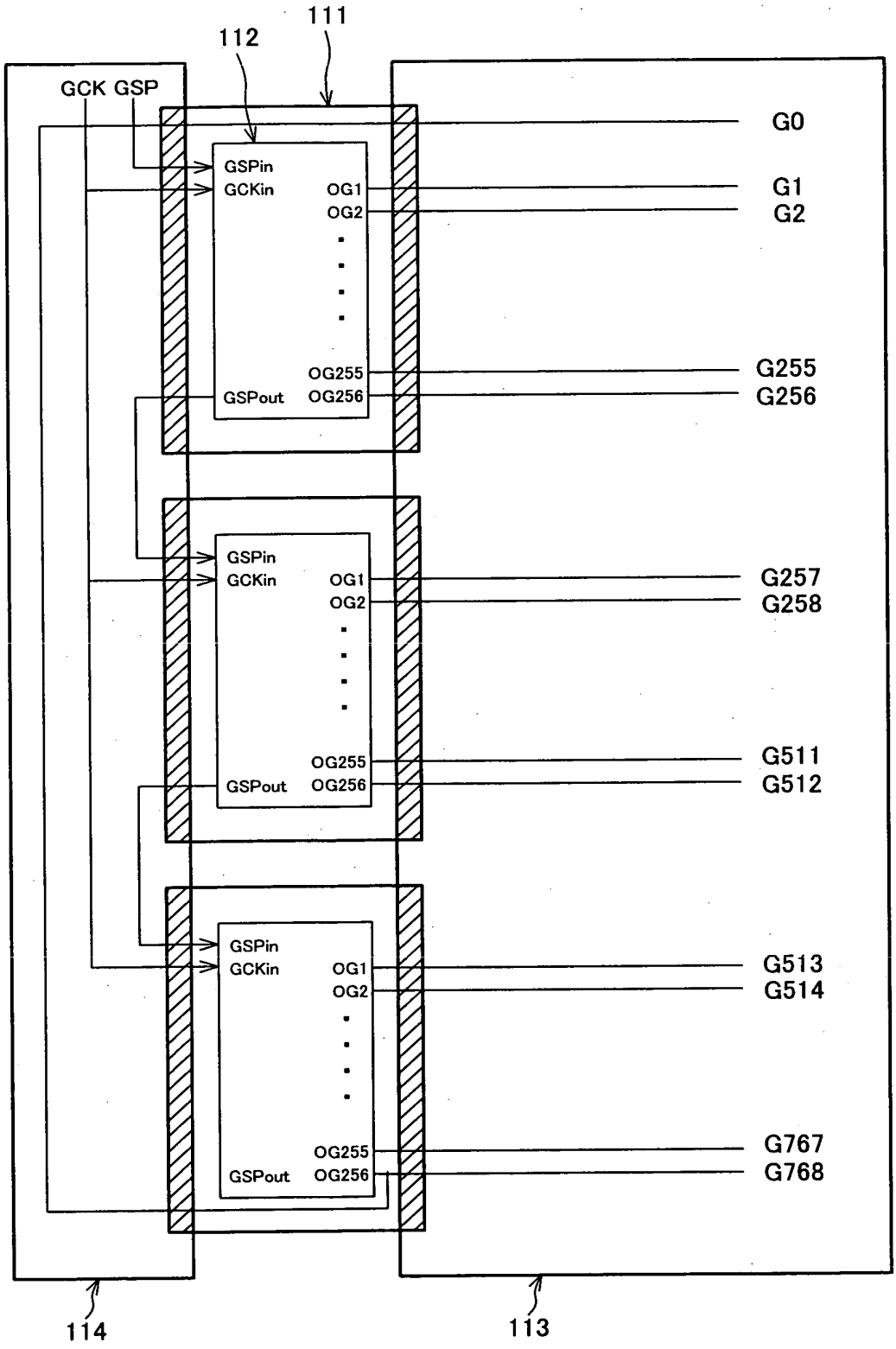

111
112
GCK GSP
GSPin
GCKin
OG1
OG2
OG255
GSPout
OG256
G0
G1
G2
G255
G256
G257
G258
G511
G512
G513
G514
G767
G768
114
113

FIG. 22

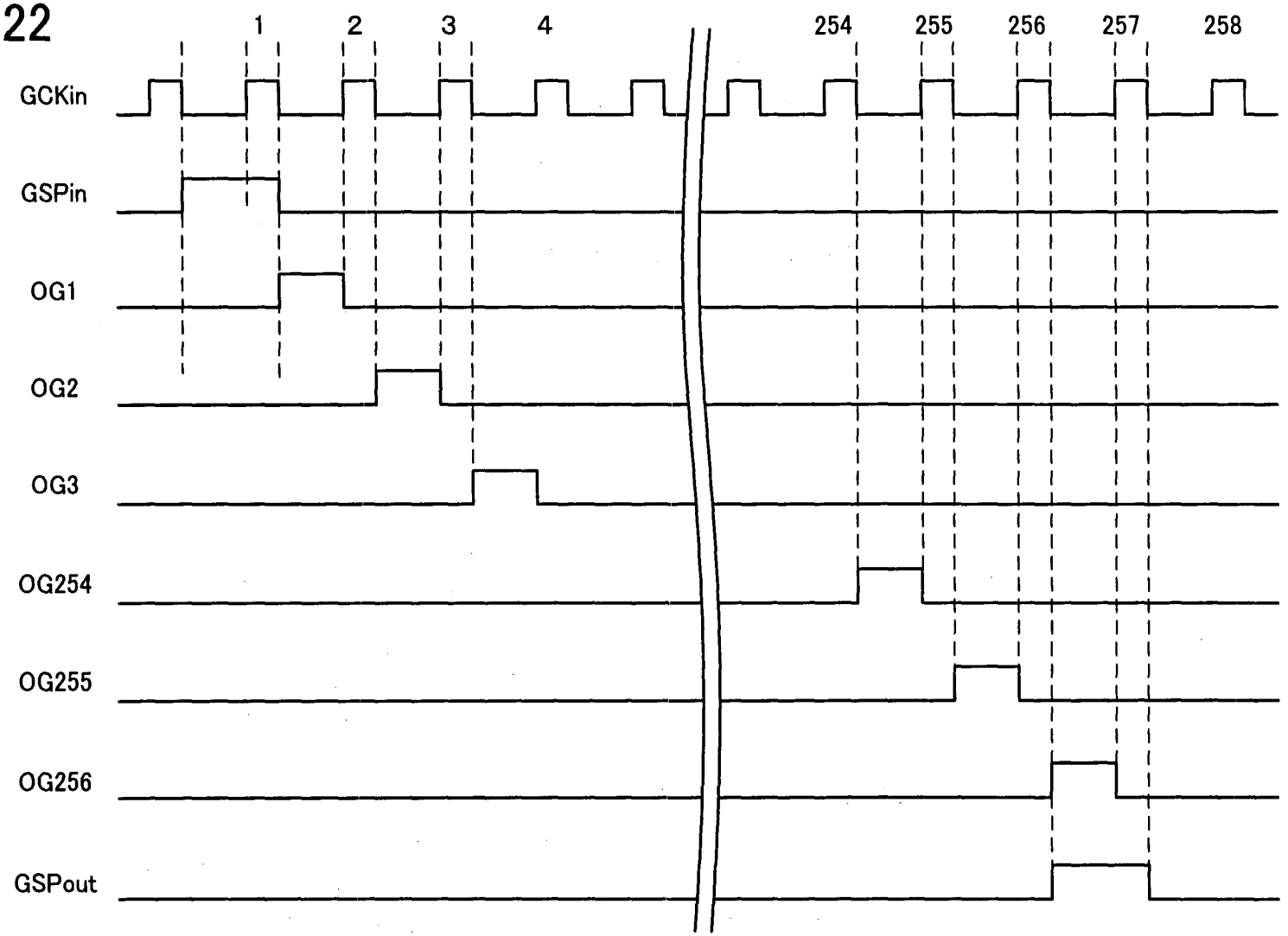

1
2
3
4
254
255
256
257
258
GCKin
GSPin
OG1
OG2
OG3
OG254
OG255
OG256
GSPout

FIG. 23

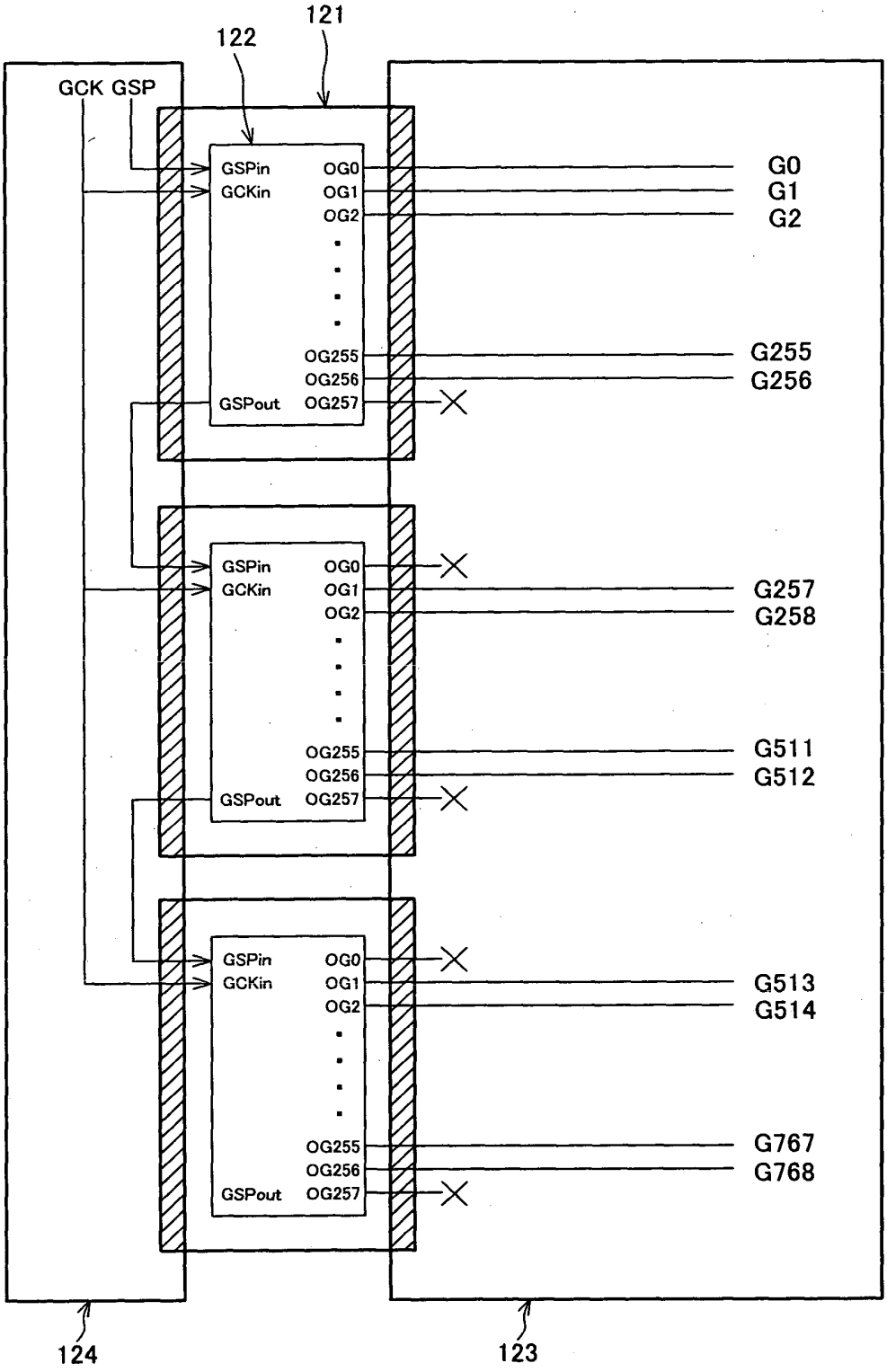

121
122
GCK GSP
GSPin
GCKin
GSPout
OG0
OG1
OG2
OG255
OG256
OG257
G0
G1
G2
G255
G256
G257
G258
G511
G512
G513
G514
G767
G768
124
123

FIG. 24

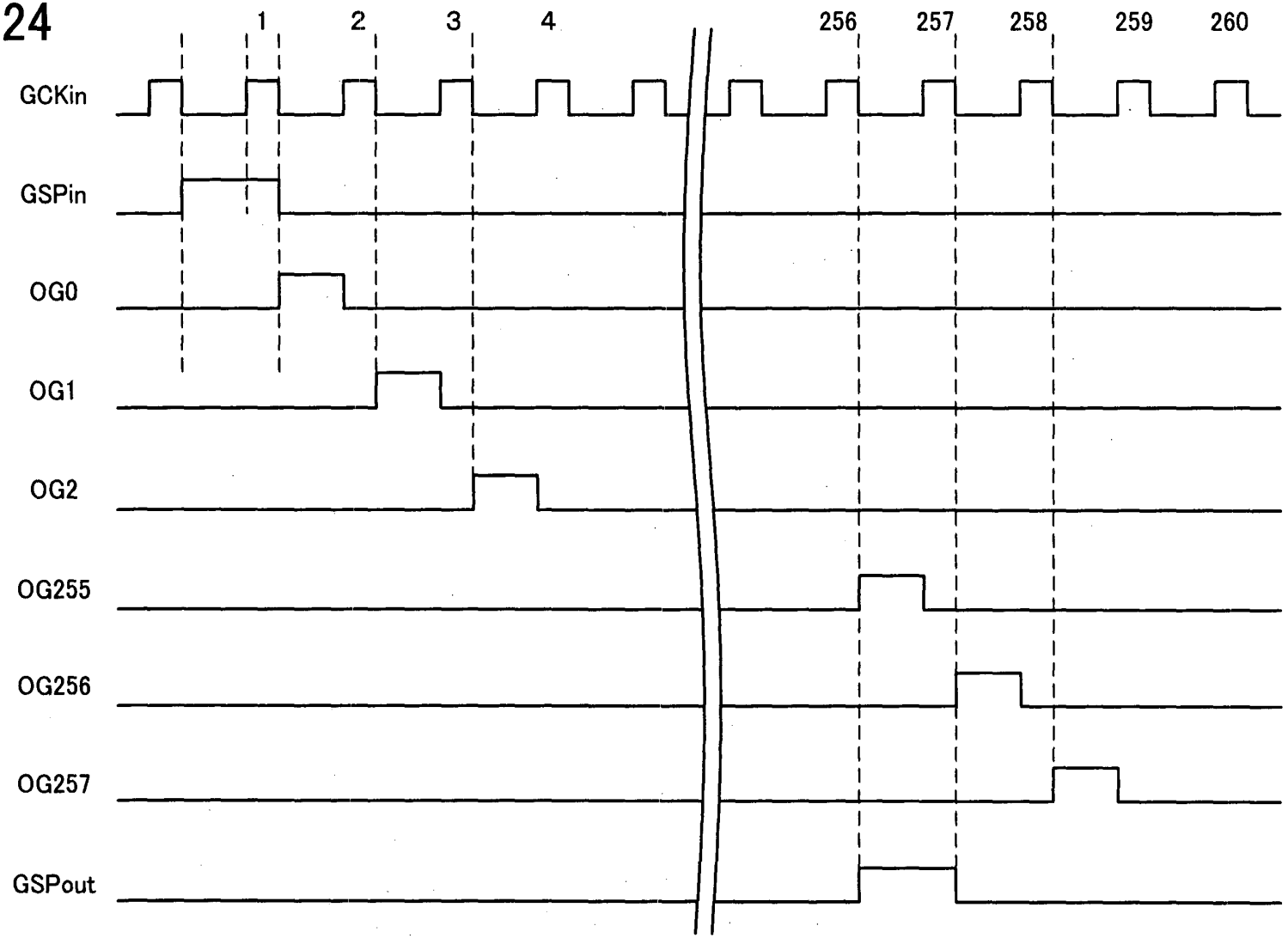

1
2
3
4
256
257
258
259
260
GCKin
GSPin
OG0
OG1
OG2
OG255
OG256
OG257
GSPout

FIG. 25

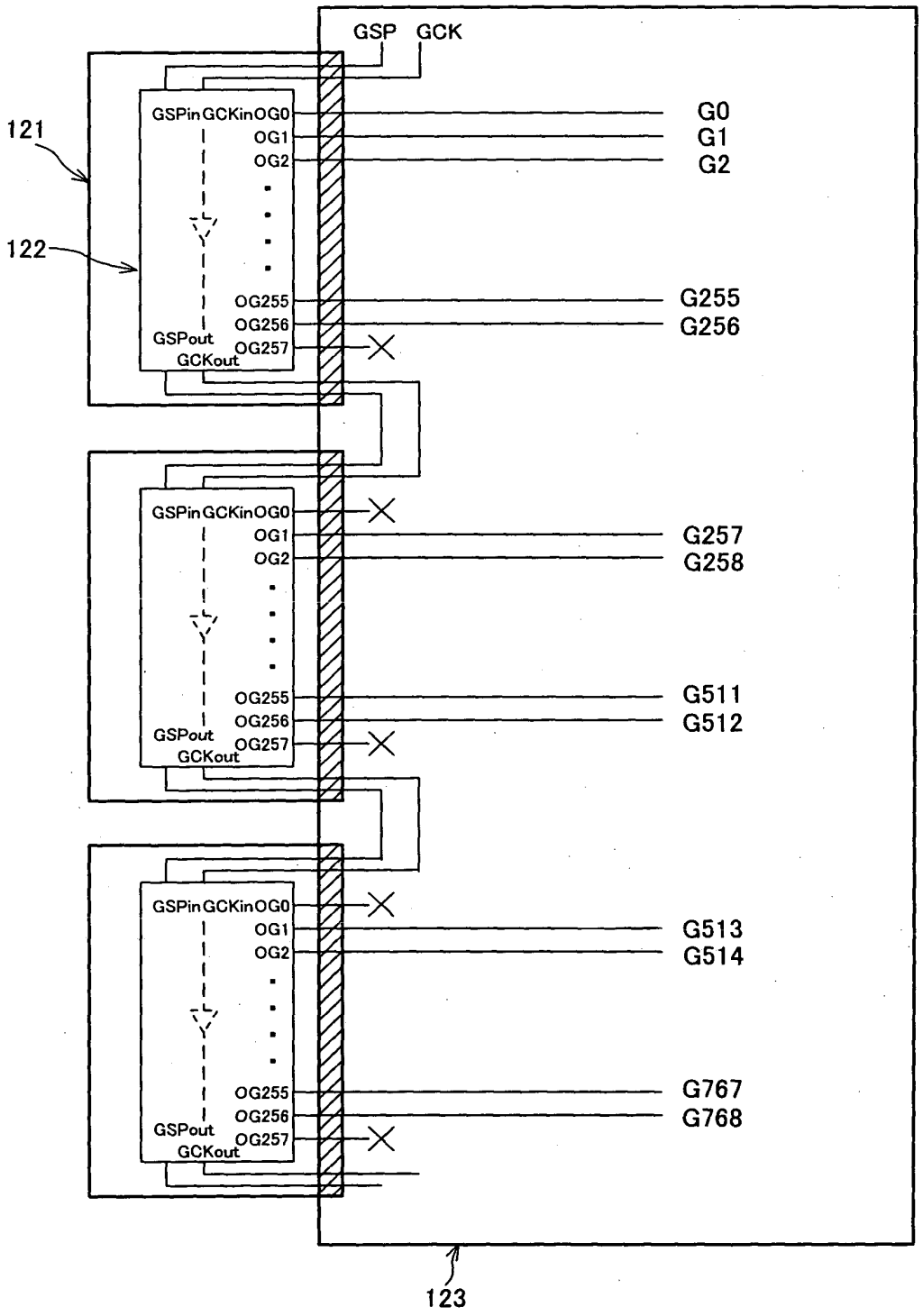

GSP
GCK
121
122
GSPin
GCKin
OG0
OG1
OG2
OG255
OG256
OG257
GSPout
GCKout
G0
G1
G2
G255
G256
G257
G258
G511
G512
G513
G514
G767
G768
123

FIG. 26 (a)

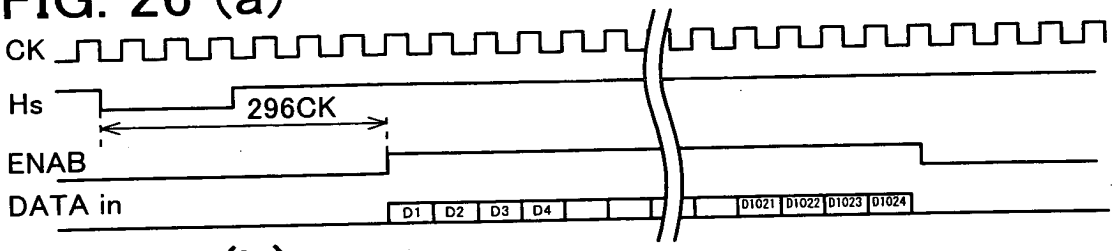


FIG. 26 (b)

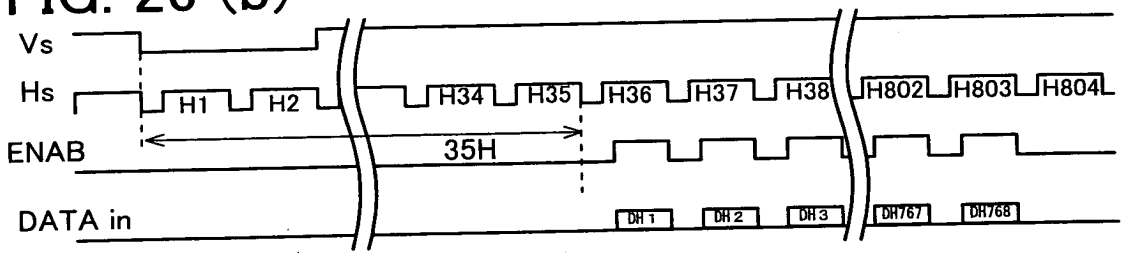


FIG. 26 (c)

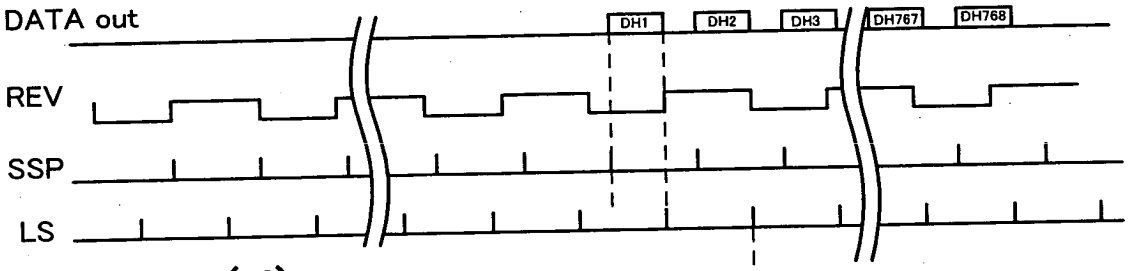


FIG. 26 (d)

FIG. 26 (e)

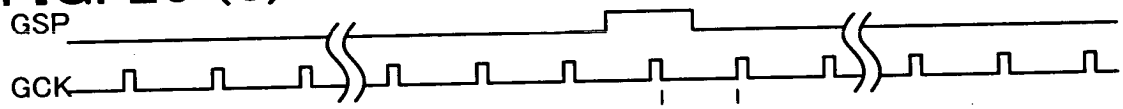


FIG. 26 (f)

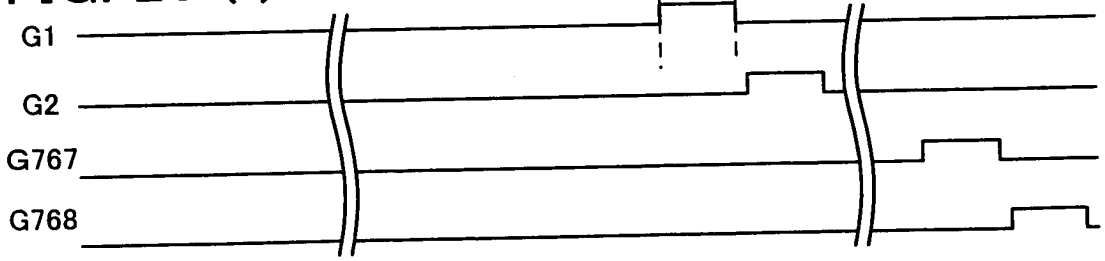


FIG. 27 (a)

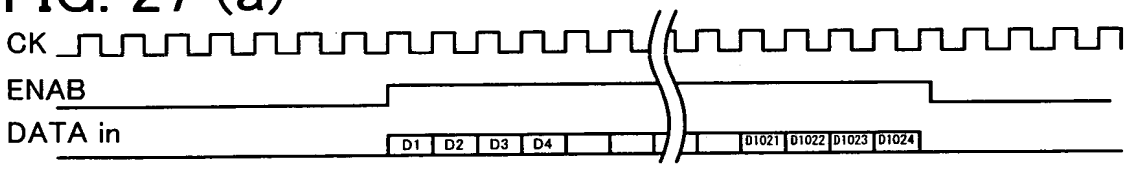


FIG. 27 (b)

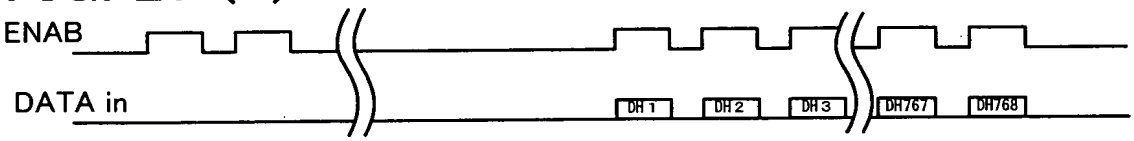


FIG. 27 (c)

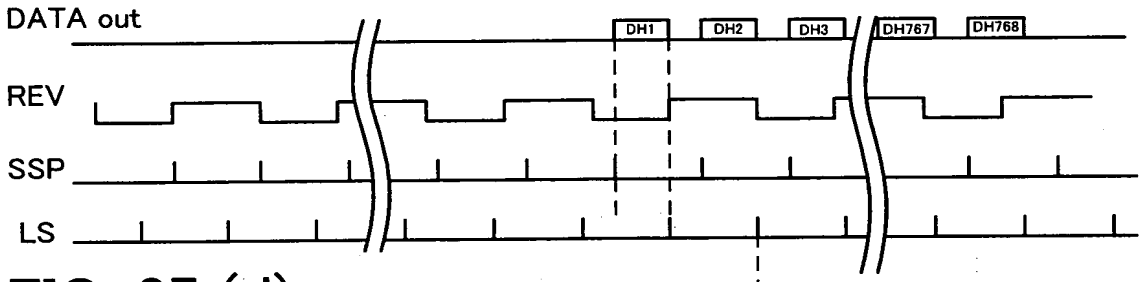


FIG. 27 (d)

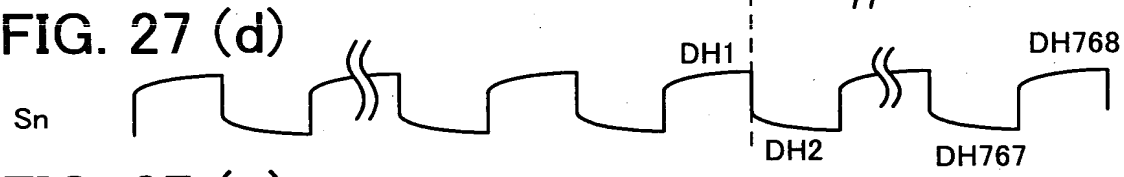


FIG. 27 (e)

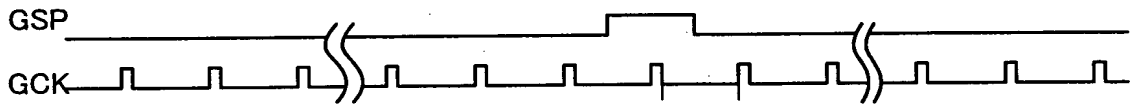


FIG. 27 (f)

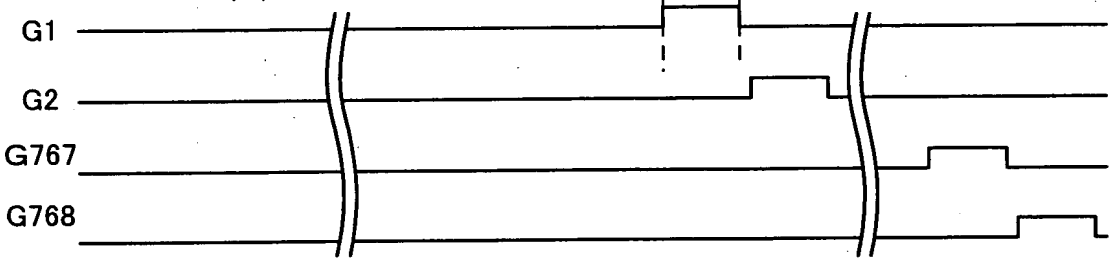


FIG. 28

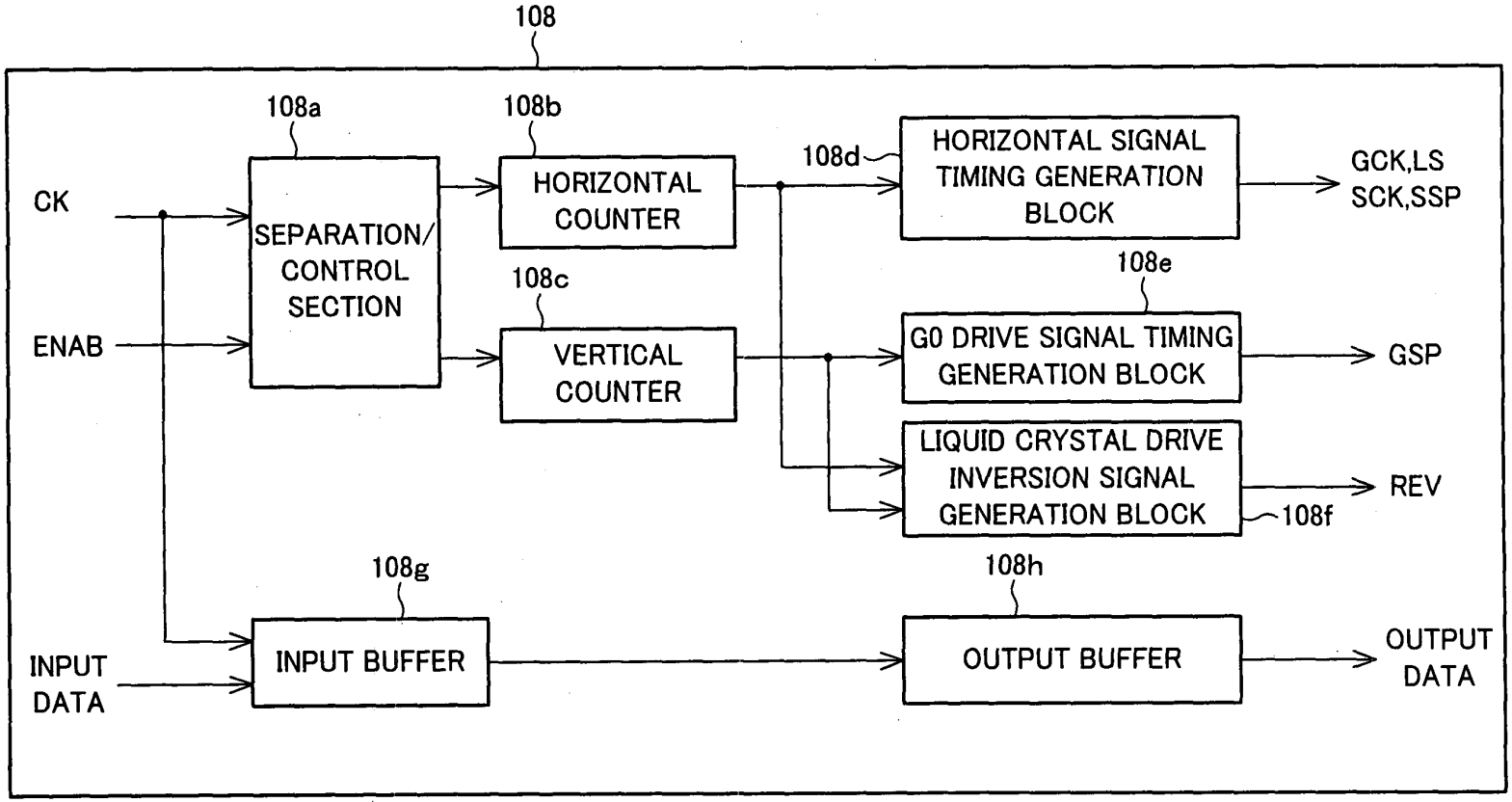

108
108a
108b
108d
HORIZONTAL SIGNAL TIMING GENERATION BLOCK
GCK,LS SCK,SSP
CK
SEPARATION/ CONTROL SECTION
HORIZONTAL COUNTER
108e
108c
ENAB
VERTICAL COUNTER
G0 DRIVE SIGNAL TIMING GENERATION BLOCK
GSP
LIQUID CRYSTAL DRIVE INVERSION SIGNAL GENERATION BLOCK
REV
108f
108g
108h
INPUT DATA
INPUT BUFFER
OUTPUT BUFFER
OUTPUT DATA

FIG. 29

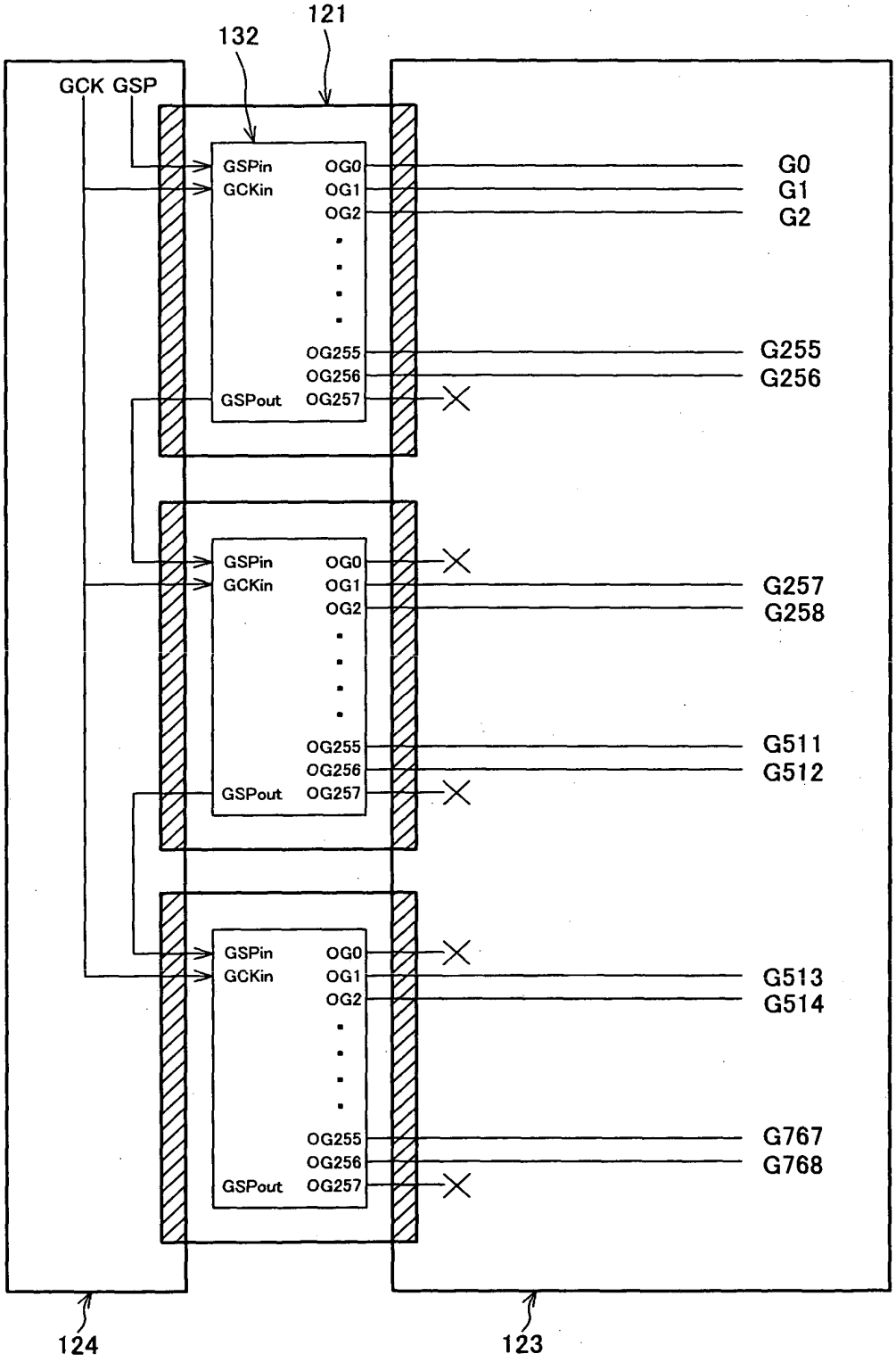

121
132
GCK GSP
GSPin
GCKin
GSPout
OG0
OG1
OG2
OG255
OG256
OG257
G0
G1
G2
G255
G256
G257
G258
G511
G512
G513
G514
G767
G768
124
123

FIG. 30

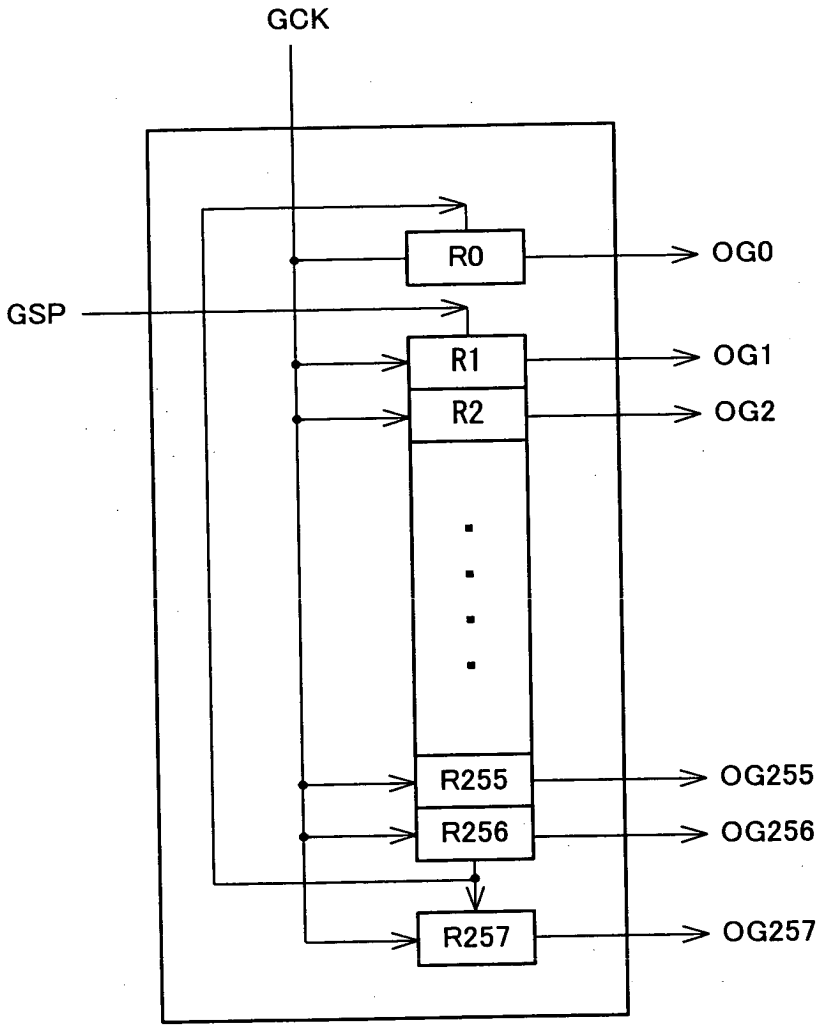


FIG. 31

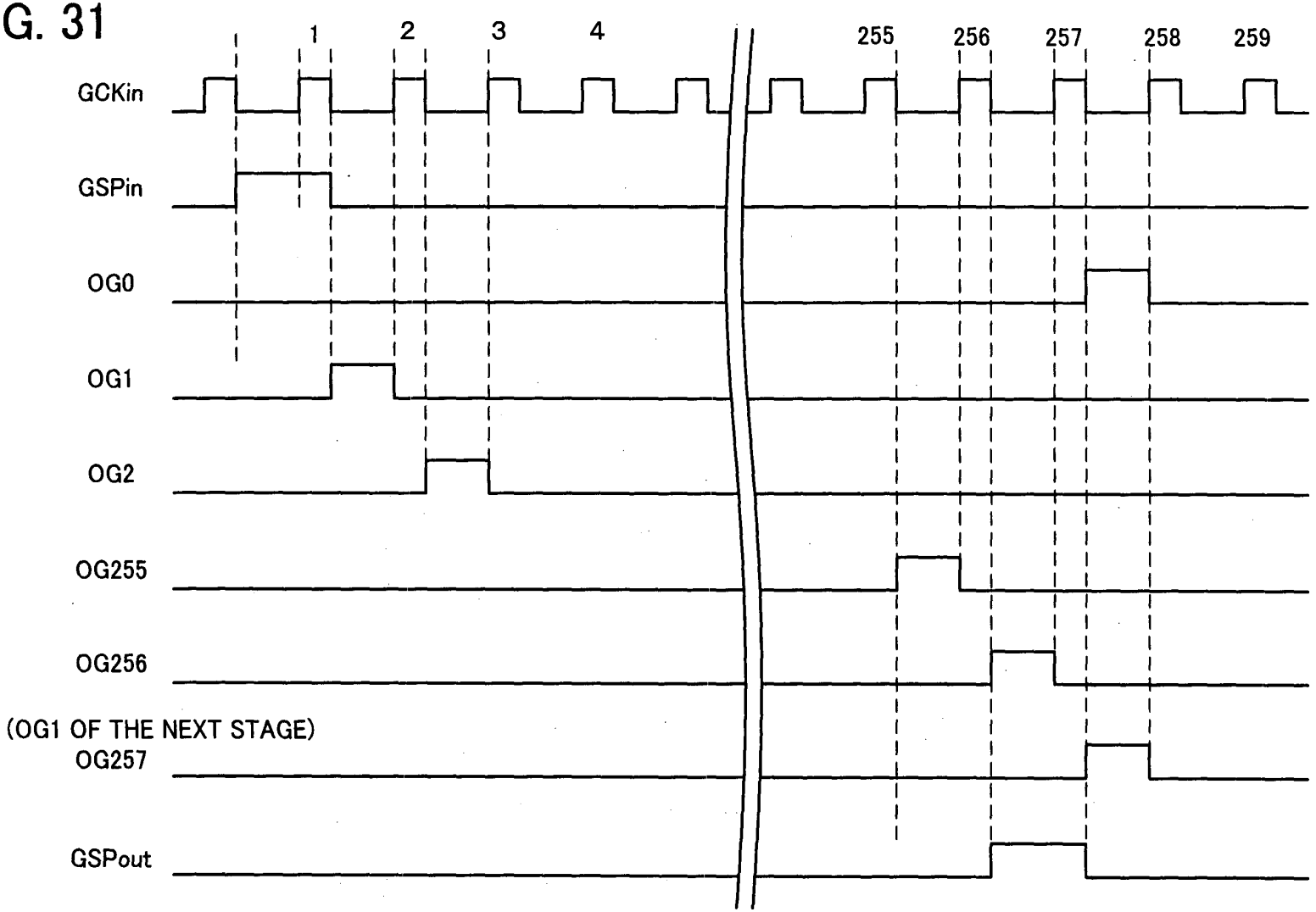

1
2
3
4
255
256
257
258
259
GCKin
GSPin
OG0
OG1
OG2
OG255
OG256
(OG1 OF THE NEXT STAGE)
OG257
GSPout

FIG. 1

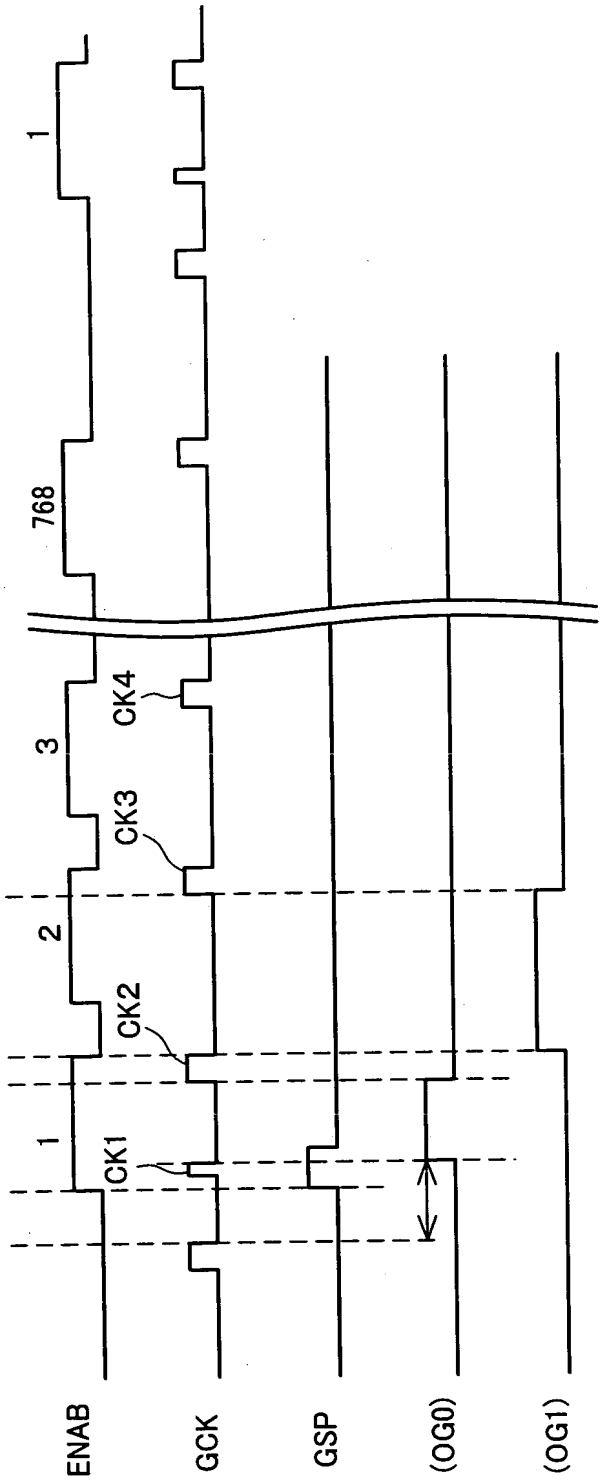
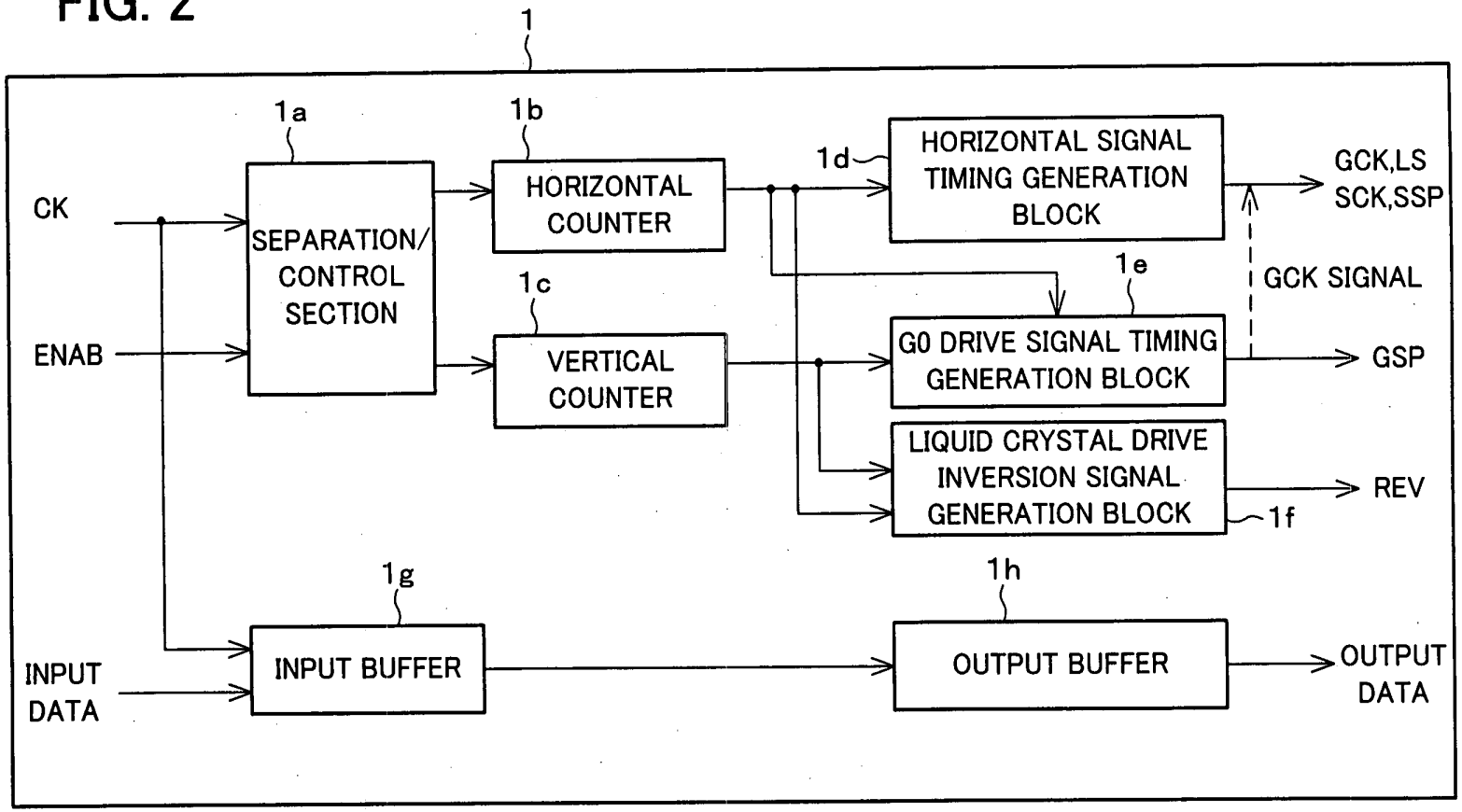


FIG. 2


1
1a
1b
1c
1d
1e
1f
1g
1h
CK
ENAB
INPUT DATA
SEPARATION/ CONTROL SECTION
HORIZONTAL COUNTER
VERTICAL COUNTER
HORIZONTAL SIGNAL TIMING GENERATION BLOCK
G0 DRIVE SIGNAL TIMING GENERATION BLOCK
LIQUID CRYSTAL DRIVE INVERSION SIGNAL GENERATION BLOCK
INPUT BUFFER
OUTPUT BUFFER
GCK,LS SCK,SSP
GCK SIGNAL
GSP
REV
OUTPUT DATA